

**University of Victoria  
Faculty of Engineering  
ELEC 499A Report**

# **The Experimental Portable EEG/EMG Amplifier**

Submitted to Dr Peter Driessen

Date: August 1, 2003

From Group 11- EPEEGAG

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In partial fulfillment of the requirements of the UVic. B.Eng. degree requirements

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Aug. 1, 2003

Dear Dr. Driessen,

Please accept the accompanying ELEC 499A project report entitled “The Experimental Portable EEG/EMG Amplifier”.

This report is the result of the ELEC 499A project that was completed in the summer of 2003. Our project group consists of Manj Benning, Stephen Boyd, Adam Cochrane, and Derek Uddenberg. We are all 4<sup>th</sup> year electrical engineering students at the University of Victoria. During this term, we worked together to design and prototype an inexpensive EEG/EMG amplifier system to be used in research as our ELEC 499A design project. A lot of our project time was spent learning about EEG/EMG signals and technologies. And still more time was spent designing and implementing a prototype module that was eventually presented at the 499A term presentations. The following report will detail the research we performed, the design specifications we implemented, and any future recommendations we have for this project.

Upon completion of this project, we feel we have gained valuable skills in signal amplification, noise reduction, circuit synthesis, and project management. These skills are essential in today's field of electrical engineering.

We would like to thank Dr. P. Driessen for offering his supervision and the group advisor, Phil Zeman for being an invaluable source of information and inspiration. The group would also like to thank UVATT for their funding contributions to our modest project. Thank you.

Sincerely,

Manj Benning  
Stephen Boyd  
Adam Cochrane  
Derek Uddenberg

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## Abstract

Mind control is no longer a mystical practice. In recent years scientists, doctors and engineers have been investigating the use of brain, and muscle tissue electrical signals to control computers. In Electroencephalogram (EEG) and electromyography (EMG), waves read of the brain and muscle tissue respectively, can be amplified and digitized to be analyzed and processed by a personal computer. Technology to acquire such signals requires low noise operation and careful design.

As a partial requirement of the B.Eng. degree, a group of students at the University of Victoria undertook a project to design and build a 10-channel Experimental Portable EEG/EMG Amplifier (EPEEA) system. The project was funded by the UVic Assistive Technology Team (UVATT).

Design specifications were agreed upon after considerable research was done on existing state of the art EEG/EMG data acquisition systems. Two main constraints on the project were a budget of \$1000 CDN and a signal range of 0-1000Hz. The upper frequency information can be used to obtain noise estimates that can in turn be used to 'clean up' the signal. This report discusses the design and approach taken to undertake such a task. Furthermore, other amplification components were researched to fully be convinced of the correct approach.

The EPEEA is comprised of six sub-systems, working to acquire the EEG/EMG signal, amplify it, and digitize it while effectively reducing the ambient noise and interference. The sub-systems are:

- Protection Circuit
- Instrumentation (differential) Amplifier
- Right Leg Driver
- Mode Switching Amplification Circuit
- Digital Backend (including the A/D converter and the USB chip)
- Power subsystem

It was concluded that the EPEEA could be built under the imposed budget constraint. However, the project members did not have time to complete a full 10-channel prototype. Instead a single channel demonstration unit was built, tested and presented. In addition to a full ten channel unit, interfacing software will be written to visualize and process the signals. UVATT hopes to apply this technology to develop a form of mind communication for fully 'locked in' disabled people.

# 1.0 Introduction

Researchers at the University of Victoria are investigating the application of **Brain Computer Interface (BCI)** technology as a substitute for other types of assistive communication. This research group is called UVATT. Their goal is to create a useable, brain-computer interface to provide completely "locked-in" persons with a means of communication. Since the group has formed, their project outlook has broadened to accommodate a large set of applications and long-term research.

One of the areas of research that UVATT has become interested in is relating a person's brain wave patterns through BCI technology with muscle stimulation and control. Both technologies are closely related and are measured with similar techniques.

For our ELEC 499A term project, we undertook a project for UVATT where we designed and tested an **Experimental Portable EEG/EMG Amplification (EPEEA)** system that measures a person's brain wave activity and response to muscle stimulation. The following report will detail the procedure we undertook to complete our project objectives. We will discuss similar measurement techniques, our project specifications, and the design methods we used to meet our project goals.

## 2.0 Introduction to EEG and EMG Signals

As discussed in the introduction, a person's brain wave patterns and muscle stimulation can be measured and recorded **using almost identical measurement** techniques. With accurate results, researches will soon be able to show a detailed direct relation between mental thought and physical motion, improve communications with lacking motor skills, and much more. But what are these measurement procedures and how are they carried out?

An electroencephalogram (EEG) test is used to monitor the electrical activity of the brain, or brain wave patterns. Electromyography (EMG) is a test that measures muscle response to electrical activity within muscle fibers, muscle stimulation. EEG signals are measured by placing several electrodes on the head around the brain. **Between certain electrodes, a potential difference is measured and converted into a waveform (EEG signal).** EMG signals are measured in a similar manner to EEG signals, but the electrodes are placed on certain body muscles. A waveform EMG signal is obtained from the potential differences measured across a muscle.

However, EEG and EMG signals are not easily obtained. This is due to the signals' electrical characteristics. They are extremely **weak signals, in the range of 1 – 160  $\mu$ Vpp for EEG and 1 – 100 mVpp for EMG.** They are band limited to a very low

frequency range, 0Hz → 100Hz for EEG and 20Hz → 200Hz for EMG. These signals are so small that they exist in the level of ambient noise. One can imagine the difficulty in measuring accurate and concise signals. These obstacles are discussed later in detail.

## 2.1 Present Day Uses and Future Predictions for EEG/EMG

Presently, there are already many uses for EEG and EMG. EEG testing can be used to diagnose seizure disorders, head injuries, tumors, causes of confusion, and a lot of other brain related abnormalities. EMG testing can be used to diagnose neurological disorders and muscle injuries. These tests have already proven to be a great benefit to the health industry, but they are just scratching the surface of this blooming technologies potential.

One of the most interesting features of EEG testing is that certain frequencies of operation determine one's state of consciousness. A few EEG wave groups are listed below.

- Beta (14 – 26 Hz) waking rhythm associated with active thinking
- Alpha (8 – 13 Hz) indicate a relaxed awareness and inattention
- Theta (4 – 7 Hz) appears as consciousness slips into drowsiness
- Delta (0.5 – 4 Hz) associated with deep sleep

One of the projects that UVATT is currently working on is an on/off signaling device based on alpha band control. This type of signaling demonstrates a high probability that a random user will be capable of intentionally generating and controlling a generic alpha band signal. This technology would provide a means of communication for persons who have lost all speech and physical motion capabilities.

Another huge area of research interest is the ability to relate mental thought with physical motion through accurate EEG and EMG observations. This technology already exists, but it is still in a very early stage of development. The main application of this technology thus far, is neurofeedback training. Neurofeedback training is a mental training method in which the patient becomes consciously aware of the general activity in the brain. This improves many mental capabilities and helps explore one's consciousness. This has huge medical applications for the paralyzed, epileptic, autistic, and others.

The future applications of EEG and EMG are as awe inspiring as they are concerning. Imagine if EEG and EMG became so precise that a computer automatically knew what you were thinking. Disabled people could communicate freely and gain motor



control from assisting robotics. Virtual reality video games could be played by simply thinking about the desired action. The list of possibilities is endless, and in time, we will likely wonder how we ever lived without this technology.

## 3.0 Project Goal and Specifications

The goal of this 499 project is to design a ten channel Experimental Portable EEG/EMG amplifier (EPEEA). Two of the main constraints are a budget of \$1000 (CAN) and a signal with a frequency range up to 1000Hz. Current state of the art EEG/EMG amplifiers were researched to help come up with the implementation specifications of this project.

### 3.1 Basic EPEEA Description

Each channel of the EPEEA will take in a differential signal from two electrodes, placed either on the scalp or the muscle tissue on the body. This signal will then be sent through a low noise, high quality differential amplifier to be amplified. Another gain stage, the Mode Switching Amplification Circuit (MSAC), further amplifies the signal. This second gain stage actually consists of three individual parallel gain stages: one for EEG, one for EMG, and one for calibration. The user, via a potentiometer, can modify the gain at the MSAC. The signal is then digitized using a sampling frequency of 8000Hz to ensure useable data at least up to 1000Hz. In the final stage there is a dedicated USB chip that sends the data to a personal computer via a USB connection that processes the digitized signal.

### 3.2 The Two Important Constraints

There are many EEG/EMG amplifier devices on the market today. Two kinds exist: one for clinical use and one for experimental use. We designed an EEG/EMG amplifier for experimental use by the Assistive Technology Team (UVATT) at the University of Victoria. UVATT chose not to simply buy an existing EEG/EMG amplifier because current ones on the market cannot perform ten channels of data acquisition for under \$1000. Furthermore, EEG/EMG amplifiers on the market do not retain signal data much higher than 200Hz. It is hoped that the signal range from 200Hz-1000Hz, which is clear of any EEG or EMG artifacts, can be used to obtain a noise estimate. This estimate can then be used in software to further eliminate noise in the band of interest, 0-200Hz.

### 3.3 State of the Art EEG/EMG Specifications

Two existing EEG amplification systems were researched to help come up with the design.

### 3.3.1 Comet Portable EEG

This EEG amplification system comes complete with a laptop computer and software to run on it. The hardware consists of 40 AC channels and 8 DC channels. The unit has an onboard A/D converter sampling at 200 or 400Hz with 16-bit resolution. Interfacing to the laptop is done via an Ethernet connection. Options include 10 additional DC channels, a video-monitoring module, and a DVD removable drive [1]. This unit cost around \$5500 US dollars not including the laptop or the additional options. The following table lists the specifications of the Comet EEG.

TS AMPLIFIER SYSTEM SPECIFICATIONS	
Input Impedance	10 Mohms
CMR	>80 dB at 50/60 Hz
Noise	<2 $\mu$ V peak to peak
Bandwidth	0.1 to 95 Hz, -3 dB
Gain	EEG 3000; ECG 1500, $\pm$ 2%
Impedance Checking	Built-in, 10 Hz sine wave. Range: 1 kilohm to 50 kilohms, 10%
Calibration	Built-in, 10 Hz square wave, 100 $\mu$ V peak to peak $\pm$ 2%
Vertical Resolution	16-bits (EEG 0.05 $\mu$ V/bit, ECG 0.1 $\mu$ V bit)
Sample Rates	200/400 samples/sec/channel, simultaneous sampling
Input Signal Range	EEG 2 mV peak to peak full-scale, ECG 4 mV peak to peak full-scale
DC Input Voltage Range	EEG $\pm$ 450 mV max, ECG $\pm$ 3 V max
Regulatory	UL2601-1, CSA 22.2#601, CE marked to MDD (93/42/EEC)
Headbox Inputs	Safety electrode inputs (32 signal leads, plus reference and ground)
Physical Specifications	Amp: 3.25" x 5.25" x 1.2", 7 oz. (8.3 cm x 13.3 cm x 3.0 cm, 196 g) HB: 3.5" x 4.5" x 1.25", 8 oz. (8.9 cm x 11.4 cm x 3.2 cm, 224 g)

### 3.3.2 A-2 Pocket EEG

This microprocessor based, hand held, standalone device can read up to 4 channels of EEG data. The data can be viewed on the LCD display or can be downloaded to a computer via infrared link to a personal computer. The channel bandwidth can be selectable at 35/40/45/60 Hz. Furthermore this device provides biofeedback for alpha band synchronicity training. Biofeedback is used to help patients generate alpha waves and control their wave amplitude levels. The Cost of this unit is \$844 US. The following table outlines the A-2 EEG specifications [2].

A2-EEG Product Specification

<b>General</b>		4-ch EEG monitor and neurofeedback with integrated Binaural Beat generator, flashing LED glasses and binocular rivalry monitor
<b>EEG</b>	Channels	4 x monopolar + reference + neutral, or 2 x bipolar + neutral (strappable)
	A->D Sampling Rate	8.196mSec (~122.07 Hz)
	A->D Resolution	10-bit precision, accuracy 9-bits or better
	Anti-aliasing filter	Switched capacitor 8 <sup>th</sup> order elliptic (r=1.2) LPF each channel, fc=programmable
	3dB bandwidth	0.5 – 35/40/44Hz (60Hz countries) selectable
	CMRR	>95dB
	Channel gain	V/V: fixed 20k, or independently Ch1/2, Ch3/4 10k-40k in 64 steps under ALC (+-20%* absolute, +-2% ch to ch) (+- 2% absolute to order); * digital potentiometer spec
	Driven Right Leg	Sum of ch common mode, mains hum suppression, current limited to IEC 60601
	Probe health measure	Measure of 2 <sup>nd</sup> stage dc offset compensation, each channel separately
	Electrodes	6 x 80-160u" silver plated casings surrounding saline impregnated sponge Expected life: >3 months usage
	Connector	8-way Modular

### 3.3.3 Specifications for the EPEEA

Based on the specifications of the previous two units (and information from the OpenEEG website) our group decided on these specifications for our amplifier system:

- 10 Channels of input (each capable of EEG or EMG)
- 16 bit quantization (minimizing quantization distortion)
- Sample rate: 8000 – 10000 samp/sec/chan
- Input impedance: 10MOhms
- CMRR > 120 dB
- Bandwidth: 0.1 to 1000Hz
- Input range: EEG(1 – 160  $\mu$ V<sub>pp</sub>) EMG(1 – 100 mV<sub>pp</sub>) ✓
- Gain: EEG gain = 86 – 110dB EMG gain = 30 – 70dB
- Signal resolution: EEG(90nV steps) EMG(92 $\mu$ V steps)

## 4.0 Alternate Amplification Systems

The differential amplification technique that we chose to use consisted of a low noise instrumentation amplifier with a high (>120dB) CMRR. To be convinced of our design we researched two other amplification systems: Hoontech's ADCIII audio amplifier, and the Cirrus CS3011 operational amplifier.

### 4.1 The Hoontech ADCIII

The ADCIII is an 8-channel analog to digital converter and pre-amp for high-end audio use. This unit takes in 8 channels of low signal on its balanced inputs, amplifies it, and then digitizes it. Low noise is crucial for this type of audio application in order to ensure that the recording unit is receiving as clear a representation of the music as possible. The following table outlines the electrical specifications of the ADCIII:

- Cirrus Logic Crystal ADC: 24bit/96kHz Delta-sigma ADC's, Dynamic Range 120dB.
- 8 channel Mic & Line preamplifiers: (Analog Devices SSM2141 -24dB ~ 50dB), 8 pre-amp control knobs.
- 8 channel phantom power supporting 48V (4 On/Off switches)
- switch for the S/PDIF output frequency rates: 44.1kHz/96kHz. This function is available when the box is used as stand-alone product.
- separate analog to digital outputs: 4 coaxial digital outputs (S/PDIF).

- 8 channel XLR inputs (+4dBu).
- 1/4" TRS stereo inputs (-10dBv).
- power On/Off switch.
- direct H-BUS connection possibility for DSP24 and DSP24 MK II.
- power: 12V 1A constant voltage.
- MIDI I/O for DSP24 on 1/8" connectors (via adapters to DIN).

To guarantee very low noise operation, balanced XLR connections are used at the inputs. Within the box the ADCIII uses an OPA627 operational amplifier to boost the low level incoming signals [3].

Balanced connections use two conductors, each of which carry the same signal amplitude but with opposing polarity. They are located inside an isolated shield, which is connected to ground. The beautiful feature of a balanced audio line is that when the signal cable is subjected to interference, that interference is equal on those two conductors but since they are out of phase, that noise is canceled and all that is left is the wanted audio signal. Our approach to cancel out the interference is to utilize a right-leg driver. This system operates similar to balanced inputs because the interfering noise signal is used to cancel itself out. Interference and the right leg driver are explained in detail in appendix I.

The Hoontech ADCIII uses a high quality operational amplifier in its pre-amplification section. This amplifier is the OPA627. One of the great features of the OPA627 is a typical CMRR of 110dB. This would be a great design feature for our application; however, the OPA627 has very bad input voltage noise spectral density at frequencies below 100Hz (shown below). This is due to the fact that the Hoontech ADCIII was designed for the audio band of 300 – 22000 Hz. Our most important signals are below 100Hz, so this amplifier is out of the question for us.

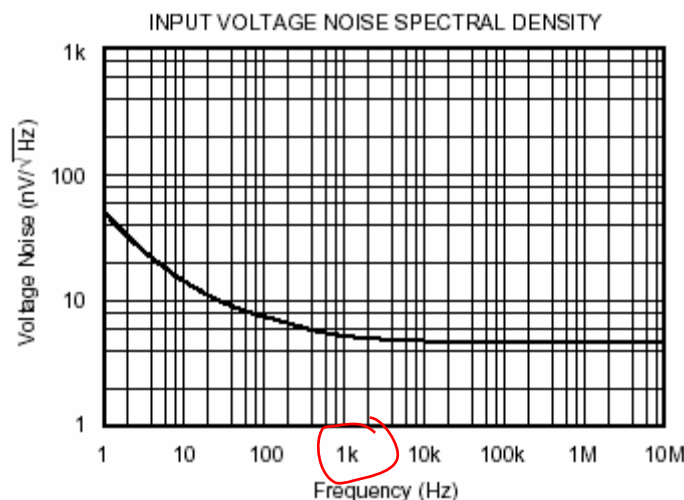


Figure 1 OPA627 Input Voltage Noise Spectral Density

## 4.2 Cirrus Logic Precision Low Voltage Amplifier

Cirrus Logic makes an excellent low voltage amplifier called the **CS3011**. This precision low voltage amplifier is rated for DC to 1kHz, exactly the frequency band specification that is required for the project. Another great feature of the CS3011 is a typical CMRR of 120dB. This meets specified requirements. But after closer inspection of the data sheets for the CS3011, one can observe the plot in figure 2 for noise power. This figure shows a large increase in noise power existing at frequencies less than about 0.1Hz. Since we require no signal distortion all the way down to DC levels (0Hz), this amplifier can was ruled out for our project. Undistorted signals at DC levels would be beneficial to EEG researchers for the possibility of added information in DC shifts or extremely low frequencies.

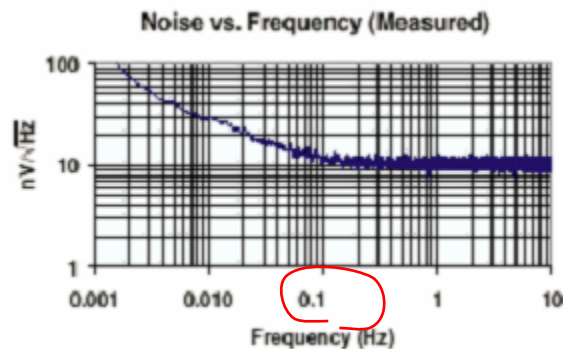


Figure 2 **CS3011 Noise vs Frequency Plot**

## 4.3 **60Hz Notch Filter**

Appendix I discusses in detail the use of a right leg drive circuit to reduce ambient noise. Another method of reducing noise is to use a 60Hz notch filter. This can be used to reduce artifacts due to the presence of power lines or transformers in the vicinity of the patient. A reasonable reduction of noise would be possible if one of these filters were used in conjunction with a high CMRR differential amplifier. However, the 60Hz notch filters are undesirable for EEG or EMG applications because the notch band, centered at 60Hz, may destroy some of the signal that researchers are interested in.

## 5.0 EPEEA Subsystems

The following six sections explain each of the subsystems of the EPEEA system. These subsystems are: The Protection Circuit, the Instrumentation (differential)

Amplifier, the Right Leg Driver, the Mode Switching Amplification Circuit, the Digital Backend including the A/D converter and the USB chip, and the power subsystem. Section 5.0 is then concluded with an explanation of the printed circuit board and the costs involved with building a prototype model of the EPEEA system.

## 5.1 Protection Circuit

The protection circuit is connected to external electrodes and is the first stop for the EEG/EMG signal entering the amplifier box. Each channel takes in two differential signals that enter the protection circuit through a pair of 2.2 k $\Omega$  resistors and three capacitors (10pF, 100pF, 100pF). This initial stage suppresses RF signals that enter the system through the electrode cables. After this stage, but before the instrumentation amplifier stage, each differential signal can be observed individually. The individual signals then enter the clamping diode section. The clamping diodes are actually a pair of matched NPN and PNP transistors that begin to conduct at voltages exceeding  $\pm 0.58V$ . With voltages above this level the transistors act as open circuits pulling all harmful currents down to ground. This protects both the user and the EPEEA. Following the clamping diodes, the signal goes through two more 2.2 k $\Omega$  resistors and enters the instrumentation amplifier. ✓

Along with its protection function, the protection circuit matches the required impedance of the electrodes. In order to prevent signal distortion, the electrodes should have impedances near 5 - 10k $\Omega$ . With input signals at the correct voltage levels, the input impedance is seen to be 6.6k $\Omega$  (three 2.2k $\Omega$  resistors in series).

### 5.1.1 Transistor Specifications

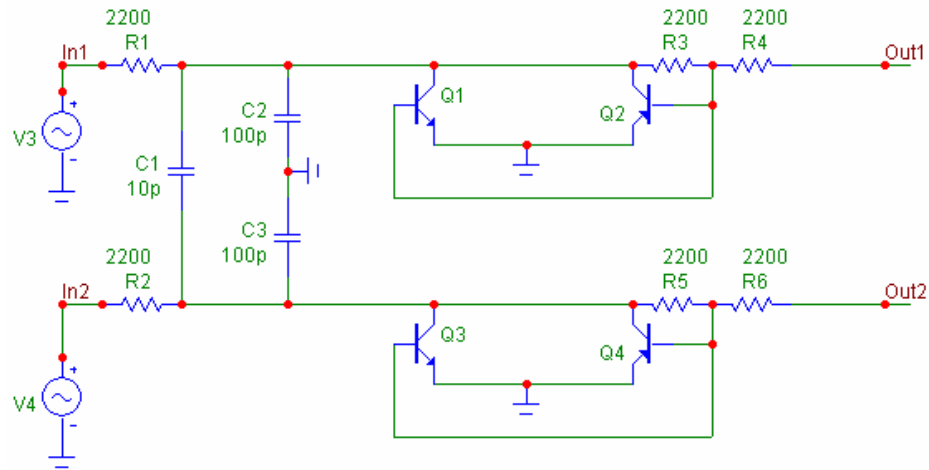
The matched pair of transistors used at this point for the protection circuit is the BC547 (NPN) and BC557 (PNP). This transistor is made by a variety of companies all offering the same specifications and price range. Important specifications are shown for each below.

**Table 1** Transistor Specifications

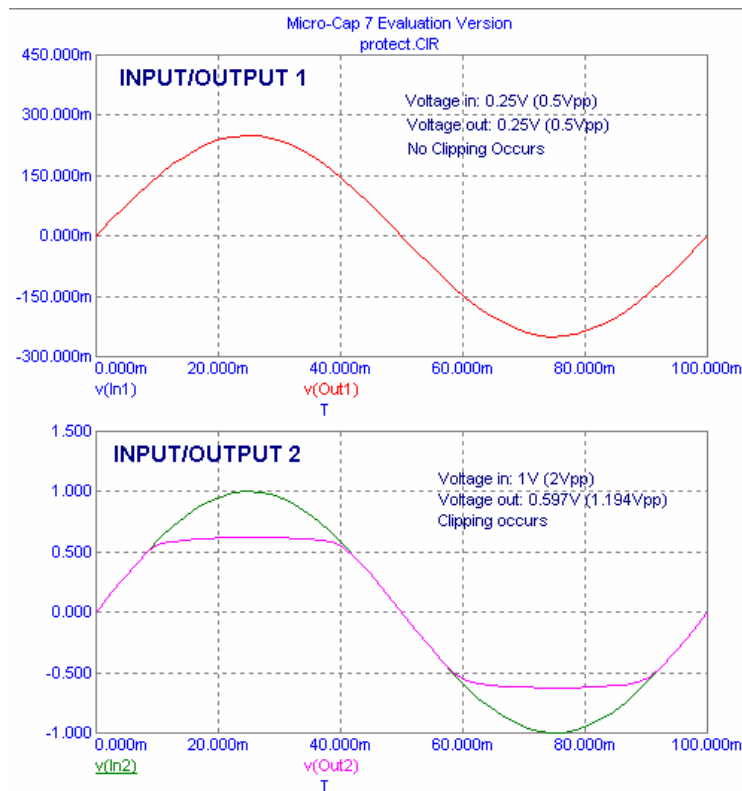
BC547 (NPN)		BC557 (PNP)	
$V_{BE(on)}$	min = 0.58V	$V_{BE(on)}$	min = -0.6V
	max = 0.70V		max = -0.75V
	@ $V_{CE} = 5V, I_C = 2mA$		@ $V_{CE} = -5V, I_C = -2mA$

### 5.1.2 Simulation

MicroCap was used to simulate and verify the correct operation of the protection circuit. The circuit was tested for three requirements: clamping voltage, frequency cut-off, and phase shift. Shown below is the tested circuit and results.



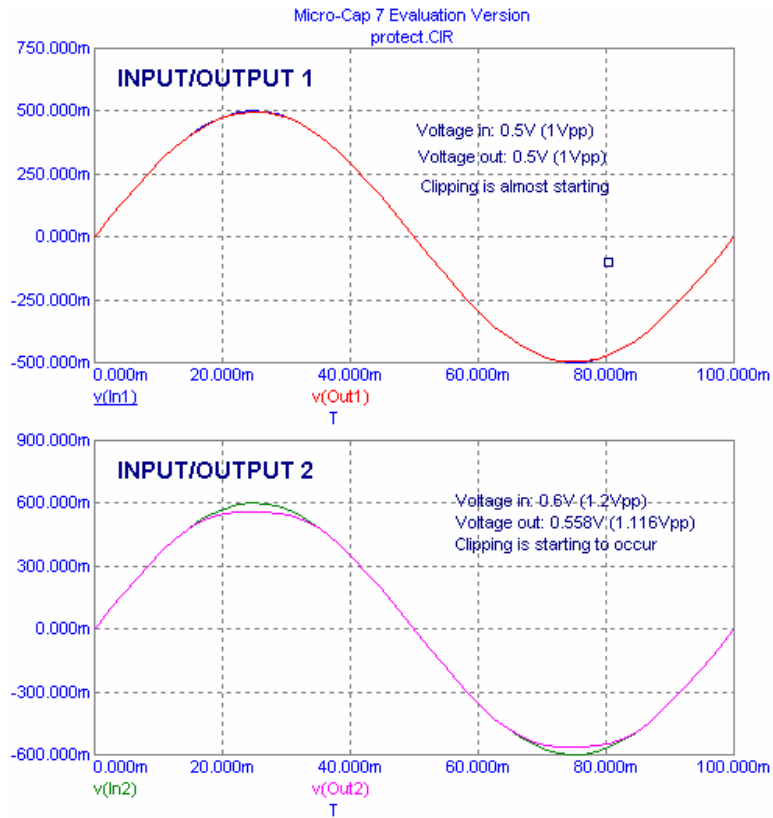
**Figure 3 Protection Circuit**



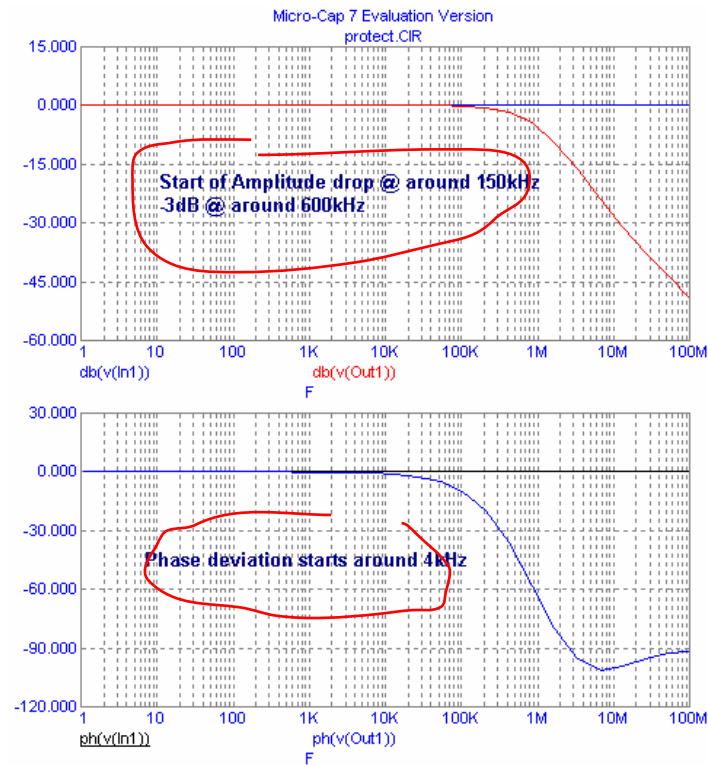
**Figure 4 A below clamping signal, and above clamping signal**

signal

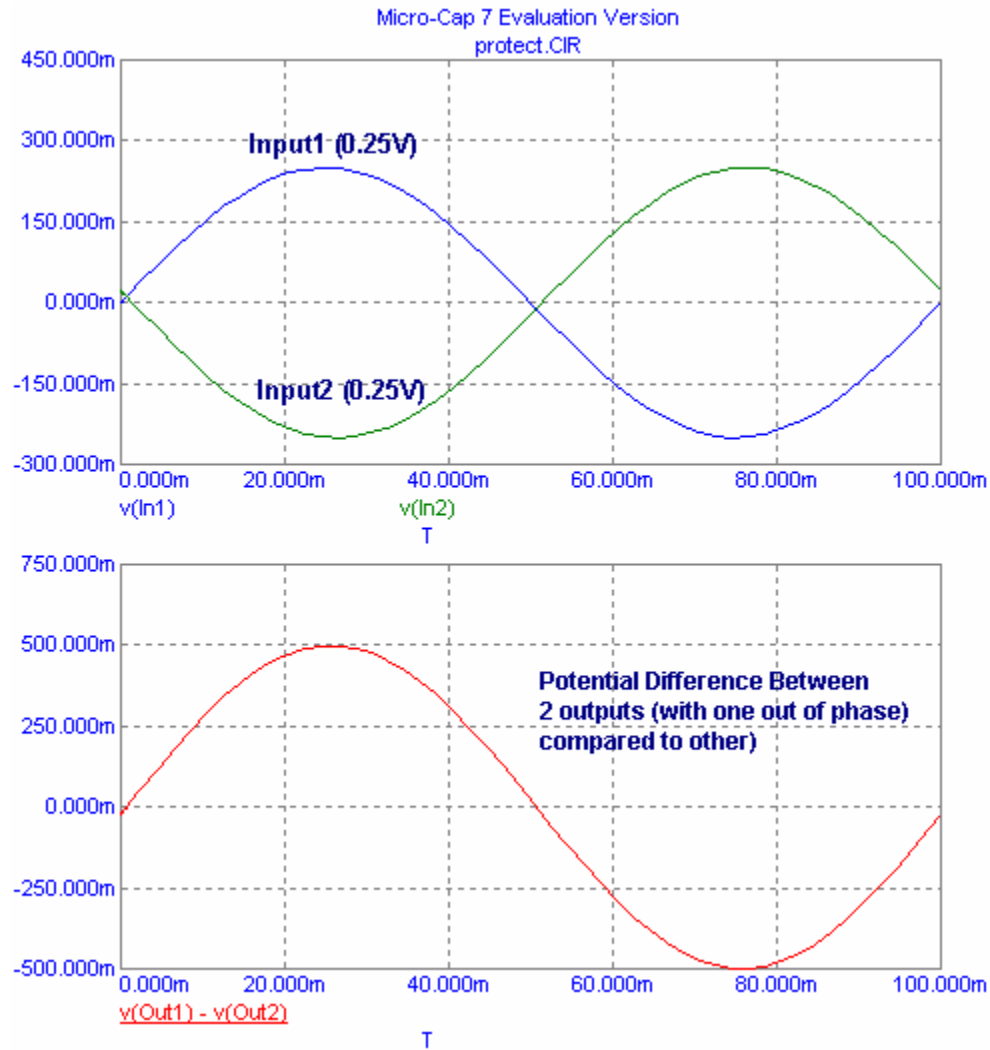




**Figure 5** *A signal just below and above clamping voltage*



**Figure 6** *Frequency cut-off, and phase shift*



**Figure 7** Un-equal phase inputs, with measured differential output

### 5.1.3 Measured Results

An identical circuit to the one tested in Microcap was connected on a breadboard and tested for the same requirements as in the simulation. The following results were measured:

**Table 2** Protection Circuit Measurement Results

Start of voltage clipping	+0.58V, -0.59V
Cut-off frequency	$f_C \approx 160$ kHz
Start of phase deviation	$f \approx 2$ kHz
Input to output resistance	6.6 k $\Omega$

#### 5.1.4 The Requirements

The requirements of the protection circuit are:

- Protect the user and sensitive circuitry without harming the input signal
- Match electrode impedance for less signal distortion
- Operate in the required frequency range

The signals of importance are  $< 100\text{mV}$  and in the frequency range of 0 to  $1\text{kHz}$ . The protection circuit passes all signals undistorted that are  $< \approx 550\text{mV}$  and  $< \approx 150\text{ kHz}$  as confirmed in the simulations and measurements. The measurements also confirmed the correct impedance match of the circuit to the electrodes. This clearly shows that the protection circuit meets our system characteristics and needs.

#### 5.1.5 Approximate Cost

Shown below is a table of approximate costs for the protection circuit of one channel.

**Table 3** Protection Circuit Cost

Approximate Costs for 1 Channel			
Part	Quantity	Approx. Price (each)	Total
2.2k $\Omega$ Resistor	6	\$0.08	\$0.48
10pF Capacitor	1	\$0.10	\$0.20
100pF Capacitor	2	\$0.10	\$0.34
BC547 NPN Trans.	2	\$0.09	\$0.28
BC557 PNP Trans.	2	\$0.10	\$0.30
		Approx. Total	\$1.60

The cost for one channel is \$1.60.

## 5.2 The Instrumentation Amplifier

Instrumentation amplifiers will be used to perform the crucial differential signal combination of the amplification stage. Due to the fact that this component plays such a large role in the retrieval of an EEG/EMG signal, a lot of time has been spent ensuring that this stage is correctly designed. Although there are many applications and types of instrumentation amplifiers, the low-signal system has proven the most appropriate method of acquiring EEG/EMG signals.

Some of the most relevant reasons for choosing this type of amplification system are as follows:

- The ability to pass DC signals. This requirement ensured that any amplification system used did not employ capacitors.
- An extremely high signal-to-noise ratio (SNR). Certain instrumentation amplifiers can now achieve common-mode rejection ratios (CMMR) of 120dB. This is comparable with even the best of the alternate amplification methods.
- Single source operation. Due to the requirements of our A/D system, the amplifier stage was subject to the use of a single rail. This method of data conversion eliminated many available active components from use.
- Low power operation. The use of a single chip rather than multiple IC's results in a power savings. This saving may become substantial with the introduction of ten independent channels.
- Proven use in similar technology. The instrumentation amplifier is commonly used in low-signal systems and has been proven to work well with this type of equipment.
- Compact design. The SO-14 package is self-contained and guaranteed to provide the results it claims. This enables a quicker start-up, less troubleshooting and minimizes the effects of residual noise effects from long connection cables.
- Price. Although relatively expensive in relation to overall cost, to recreate this component could not be done in a cheaper fashion with passive components.
- Availability. This item can be delivered within two business days.

The instrumentation amplifier could be considered the most important component of the EEG/EMG device. Due to this fact, further explanation is warranted into the inner workings of this device. It is this stage that controls the essential combining of the differential input signals and sets up the common-mode rejection ratio for the entire device. It is also the instrumentation amplifier that must deal with the issue of noise in the incoming signal since the output signal is usually large enough to reduce this effect. After considerable investigation, the INA114BU instrumentation amplifier from Texas Instruments was determined to be the best integrated circuit available.

## ✓ 5.2.1 Instrumentation Amplifier Basics

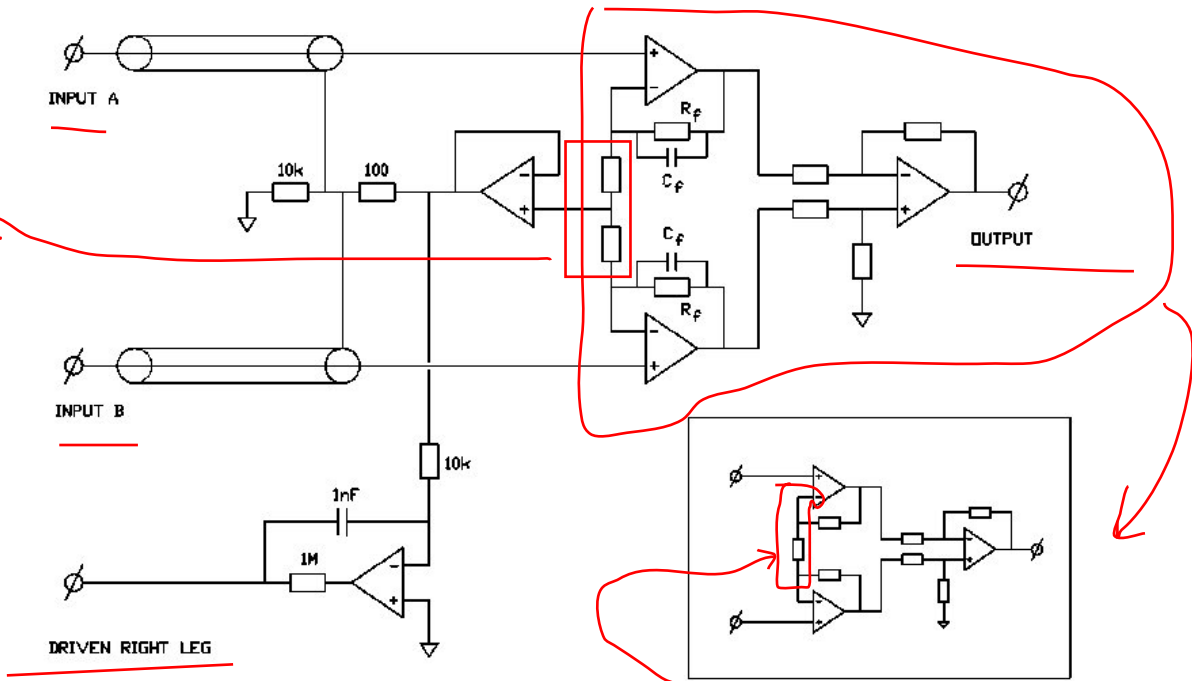
An instrumentation amplifier performs a combination of important tasks in the modification of an analog signal. Firstly, this amplification stage takes in two separate signals and relates them to each other. This relation is known as the differential signal. This differential signal allows for the two input signals to vary in polarity and amplitude. It also allows for the signals to possess a common DC signal that will not be introduced into the resultant output. For this reason, a floating ground, such as exists in a human, is acceptable in relation to the input signals.

Furthermore, an instrumentation amplifier is realized through the integration of a series of three op-amps. This construction method ensures, by default, that the differential signal must be referenced to the op-amp output zero voltage. This reference now guarantees that the unknown common-mode DC signal found in the input signals is eliminated and the output is a pure differential signal related to the board ground plane. As a bonus, the INA114BU allows for the op-amp output voltage to be referenced to a variable voltage. This ensures that the differential signal will continue to remain referenced to this signal throughout the entire board and no unintentional DC offset will be obtained later in the system.

It is also the job of the instrumentation amplifier to remove noise from the input signals. This concept is closely related to the previous comments about common DC signals. Over time, the human, and therefore the input signals, are subjected to variable Interference currents from a variety of sources. This noise causes the floating potential of the human to randomly fluctuate up and down. Due to these fluctuations, a common-mode signal is introduced into the instrumentation amplifier, which in turn creates erroneous results to be produced at the op-amp output. There exists an interesting method of counteracting this fluctuation in the form of a Right Leg Driver. This topic will be discussed in its own right after the Instrumentation Amplifier section.

Finally, the obvious other job of the instrumentation amplifier is to amplify the differential signal. The INA114BU allows for variable gain from 1 to 10000 times dependent on an external resistance.

## 5.2.2 Low Signal Instrumentation Amplifiers



**Figure 8** Biomedical instrumentation amplifier

(Equipped with guarding and driven right leg circuits, based on the three operational amplifier instrumentation amplifier).

An instrumentation amplifier consists of two variable-gain op-amps and a unity-gain differential amplifier. For low-signal applications, the negative inputs for the variable-gain op-amps are tied together via matching resistors, and a floating ground is created. The floating ground is actually dependent on the combined outputs of the variable-gain op-amps and therefore also directly related to a known board reference ground. This floating ground allows the second stage differential amplifier to achieve CMRR values from 10-50dB higher than conventional instrumentation amplifier models while the two matching resistors set up the initial gain value. The variable-gain op-amps act as voltage followers (due to the floating ground) and the common-mode gain equals 1. The typical instrumentation amplifier is shown in the inlay above and can be bought as an IC chip that may or may not consist of the  $C_f$  capacitors. In the picture above however, the  $C_f$  capacitors should not affect the DC component of the signal and are used to remove AC signals.

ground is variable

For the first stage of the amplifier, the op-amps act as adjustable gain voltage followers and the common-mode gain equals one. So,

$$A_v = R_2/R_1 + 1$$

$$A_{cm} = 1$$

Remember,

$$\underline{CMRR = A/A_{cm}} \quad \text{or} \quad \underline{CMRR_{dB} = 20 \log(CMRR)}$$

So obviously the common-mode gain,  $A_{cm} = 1$ , is as good as we could hope for!

Now, it is the second stage differential op-amp that controls the CMRR of the instrumentation amplifier.

OR — Due to the rules of a differential amplifier, this system acts like a Wheatstone bridge. The difference in the four resistors becomes the system downfall. The gain is  $A_v = 1$  as all of the resistors are of the same value, and the common-mode gain  $A_{cm} = \pm 2 \Delta R/R$ .

The issue then becomes how closely matched the resistors can be. For example, for 25000 ohm resistors (although it can be any size resistors) that are  $\pm 0.1$  percent, the CMRR becomes a minimum of 54dB through the following:

(2)

$$A_v = 1 \quad A_{cm} = \pm 2 \Delta R/R \quad R = 25000\Omega$$

$$CMRR_{dB} = 20 \log \left( \frac{2 \times 25000 \times 0.001}{25000} \right) = -53.979$$

$A/A_{cm}$

For  $\pm 0.01$  percent, it becomes a minimum of 74dB and so on. The issue now becomes how accurately one can match the four resistors needed in the differential amplifier circuit.

It is this matching issue that became the driving reason we chose the INA114BU instrumentation amplifier IC chip. It has an available gain from 1 to 10000 as previously stated, and a CMRR of 115dB ( $CMRR \cong 562000$ ), which means the resistors must be within  $\pm 8.89e-5$  percent of each other! This amazing consistency is established through a laser cutting technique of the IC resistors. Since we would never be able to find surface mount resistors of this accuracy, the INA114BU chip option became quite viable.

After investigation, the INA114BP chip became the component of choice due to all of the previous considerations and its remarkable noise performance of  $0.4\mu V_{p-p}$  from 0.1 to 10Hz. Other features of this chip are the low drift current of  $0.25\mu V/^{\circ}C$  max,

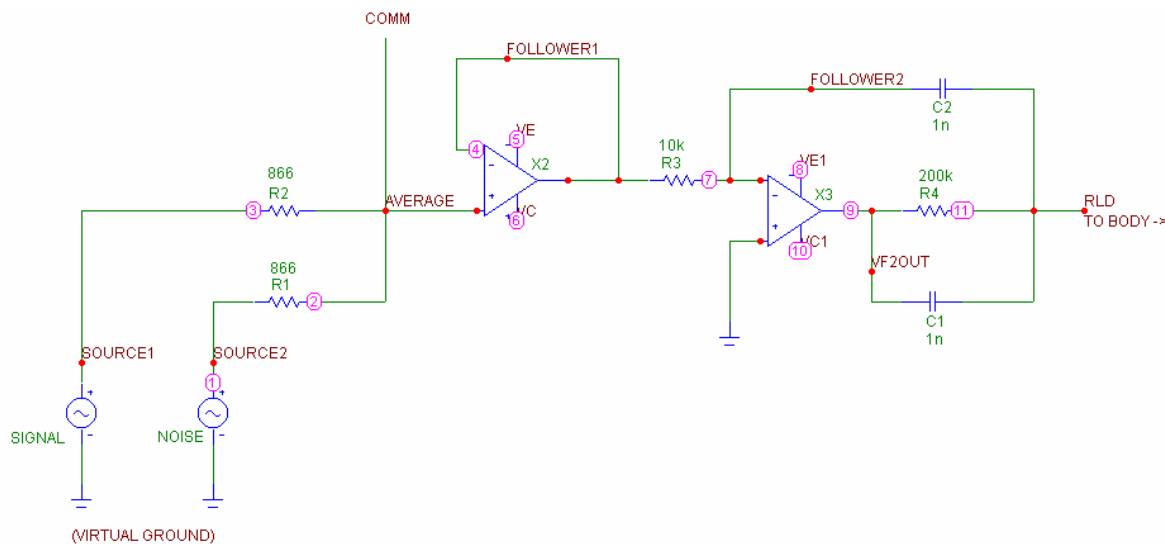
low quiescent current of 3mA max, and slew rate of 0.6v/ $\mu$ s. These chips cost around \$11.00 each and one will be needed for each channel. Although this is quite a substantial overhead for the project, it is the most crucial component and the extra money spent will reflect that fact.

With the decision made on the instrumentation amplifier, the floating ground became the issue. Investigation has led to the design and testing of a feedback network that actually feeds voltages back into the body in an attempt to minimize the common-mode signal. This network is called the Right Leg Driver.

### 5.3 Right Leg Driver

The Right Leg Driver (RLD) is used to raise the common-mode rejection ratio (CMRR) of the instrumentation amplifier. With this higher signal-to-noise ratio (SNR), the differential signal obtained is ensured to possess only relevant information and a minimum of Interference currents or irrelevant data. The idea behind the RLD is to maintain a known voltage potential in the human subject that is directly related to the system board ground. This method then reduces the common-mode DC offset previously found in the system and thereby attempts to cancel any different DC offsets that individual channels or probes may experience.

The actual method of the RLD is quite unique. A feedback network is created that depends on the averaged inputs from the combined instrumentation amplifier floating grounds and a GROUND signal originating from the human (see Appendix). This signal is then sent through an inverting gain stage that completes the feedback loop, which effectively counteracts any potential changes in the subject. A schematic layout has been reproduced (as shown) in Micro-cap for testing purposes.



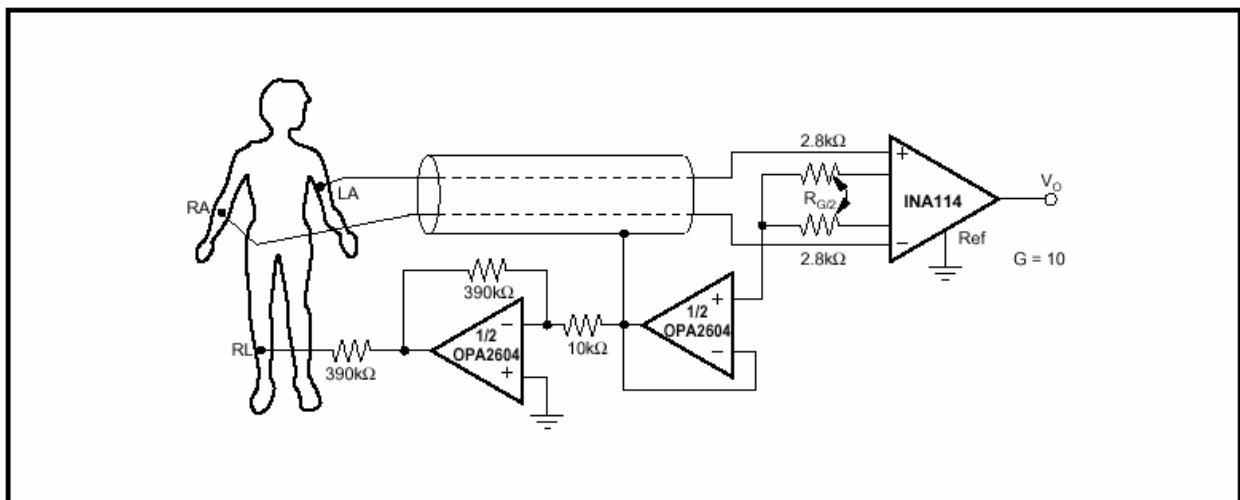
**Figure 9** Reproduction of the EPEEGAG Right Leg Driver circuit in Micro-cap



To fully understand the Right Leg Driver, it is necessary to appreciate the influences that derive its requirement. Therefore, please refer to the [attached article](#) *Interference and the Right-Leg Driver*. This article has been created as a conglomerate of interesting articles, textbooks and observations that fully encompasses the development of the RLD.

This method of reducing the CMRR is actually quite common in small signal applications. In developing the INA114BU, Texas Instruments (TI) has actually developed its' own version of a compatible RLD system as shown below. This application method however did not seem to meet the requirements of our system and it was further developed.

### 5.3.1 RLD Development



**Figure 10** Recommended RLD system as shown in the INA114BU datasheet

As can be seen in both the attached article *Interference and the Right-Leg Driver* and in the figure above, the first part of the RLD is an averaging circuit. The system above has been developed by TI in an attempt to average the two negative inputs to the instrumentation amplifier and therefore balance the floating ground. These resistor pins usually just set up the gain of the INA114BU, but in RLD applications, the values are halved and utilized as shown. The RLD tap into this circuit can then be brought off this floating ground in such a way that does not bias the amplifier with any adverse effects.

The next component in the circuit would be the voltage follower. The simple purpose of this op-amp is to ensure that there is no loading or feedback signal placed onto the instrumentation amplifier. Depending on which RLD model is chosen, the output of

this op-amp would be where you attach any cable shielding for the electrodes. There is then a 10k $\Omega$  resistor separating the op-amp output from the next stage.

The third stage of the RLD is a common carrier or averaging stage, which we will call COMM for simplicity. All of the RLD circuits of the device are joined to this COMM line which then forces COMM to an average potential based on the various outputs of the RLD voltage followers. To this average potential (COMM) is also connected an electrode from the human which acts as a human ground reference. At this point, COMM has multiple averaged inputs all attached to the human ground. Also, COMM is referenced to the floating ground of the instrumentation amplifier via an op-amp. In turn, the op-amp is referenced to the board ground and therefore fluctuates around some midpoint potential based on the op-amp characteristics. This combination leads to a known potential relation between the human ground and the board ground thereby eliminating the common mode signal.

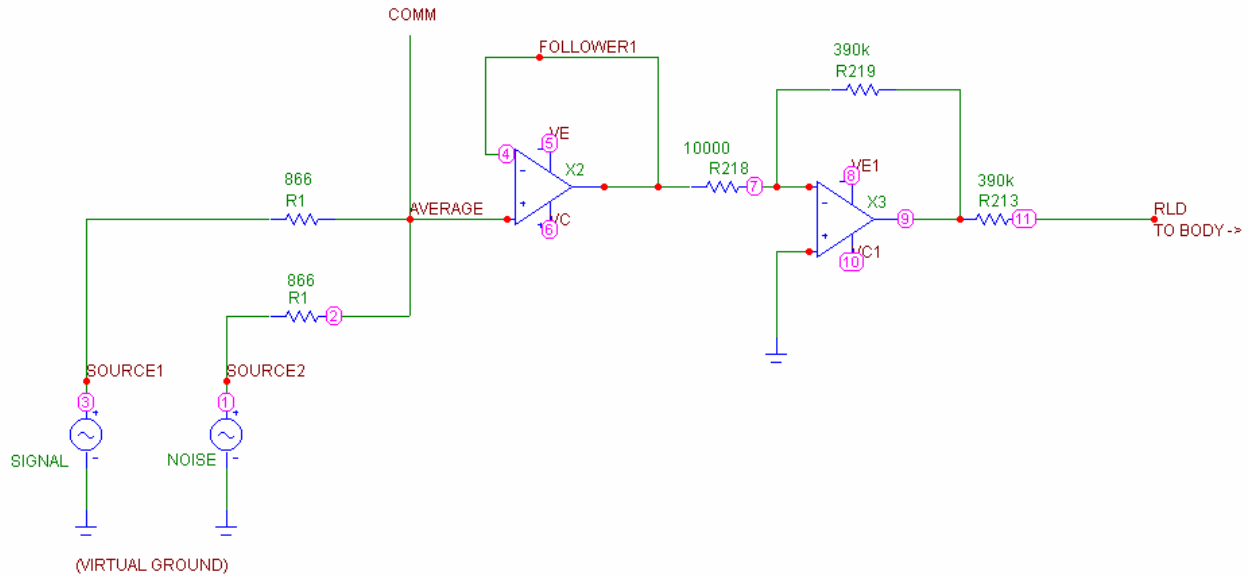
This system would be perfectly acceptable if it were not for the constant fluctuations and influence of Interference currents. Due to this influence, the human ground potential varies up and down which in turn creates variable DC offset signals and a decrease in the CMMR. In order to counteract this problem, a clever feedback loop is created that ensures a constant relation to the board ground.

The COMM signal is fed through the negative input of an op-amp and through a large gain stage. This high gain is necessary as the immediate influence of Interference currents does not normally effect the potential of the human in the order of volts, but merely in the milli to microvolts range. The negative feedback loop therefore counteracts the influence of Interference currents and ensures the stability of the human ground to that of the board ground. This assurance guarantees high CMRR values from the instrumentation amplifier.

### 5.3.2 EEG/EMG Right-Leg Driver Improvements

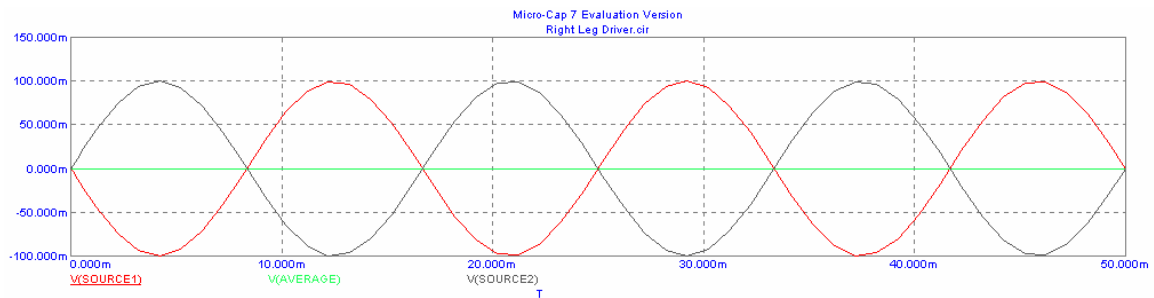
As stated previously, the method that TI used to implement a RLD did not match our requirements and the method shown in Figure 4 of the attached *Interference and the Right-Leg Driver* article was implemented. This version of the RLD was chosen after careful observation in Micro-cap as shown.

Initially, the Right-Leg circuit was developed as shown in the TI datasheet. This is shown below:



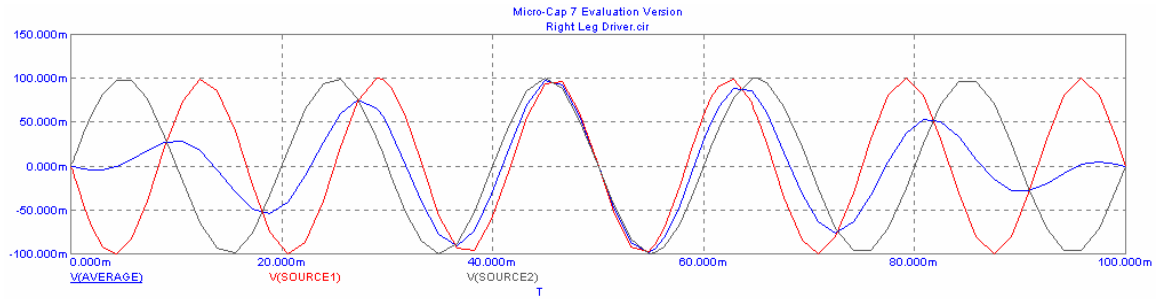
**Figure 11** *Reproduction of the TI version of the Right-Leg Driver*

The circuit was tested as follows. First, by placing both a positive and negative signal through Source1 and Source2 respectively, the concept of the average COMM signal was tested.



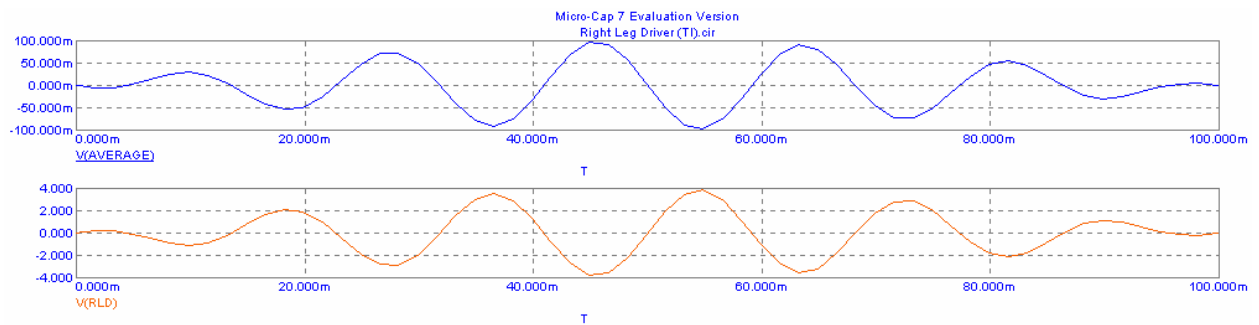
**Figure 12** *Signal Averaging*

As can be seen, the signal is cancelled out (averaged). Now knowing that this worked, a new signal was created to mimic a noisy common-mode signal.



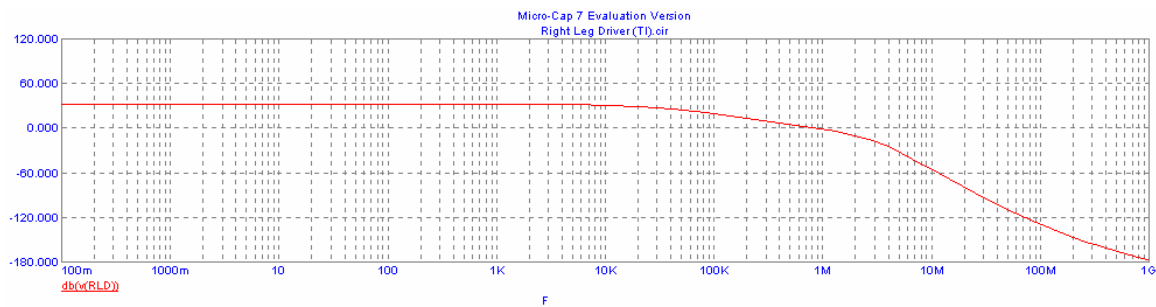
**Figure 13** Noisy Common-Mode Signal

This noisy signal was then used to drive the circuit using the recommended TI component values. The output signals are shown in the figures below. As can be seen, the average input signal corresponds to the inverse of the RLD output as desired.



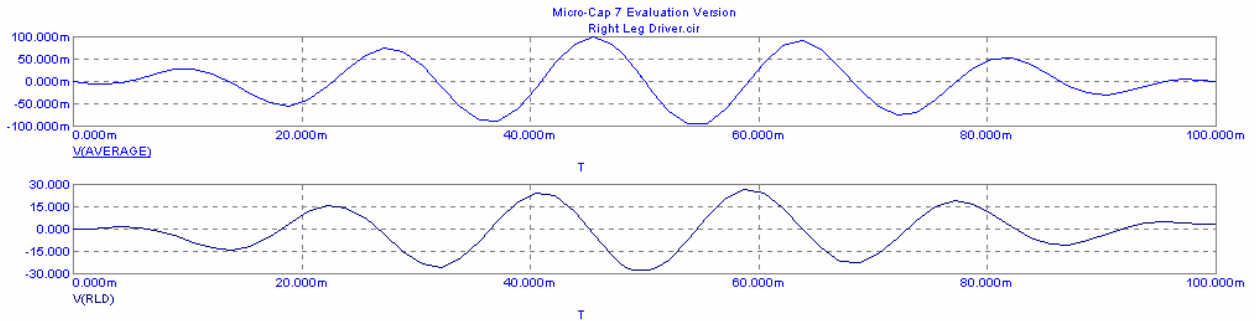
**Figure 14** TI RLD output signal

The right-leg driver gain is calculated to be  $A = -39$ , as can be seen, which is not nearly high enough. Although this gain value is easily changed, it is the frequency response, which causes the most concern. The roll-off does not significantly reduce until the megahertz range which will allow any high frequency noise found on the COMM line to have an equal gain value. This equal gain model could feed back into the human subject and cause a possible oscillation in the op-amp that would continue to grow in amplitude until it rails, rendering the RLD useless. This model needed to be redesigned.



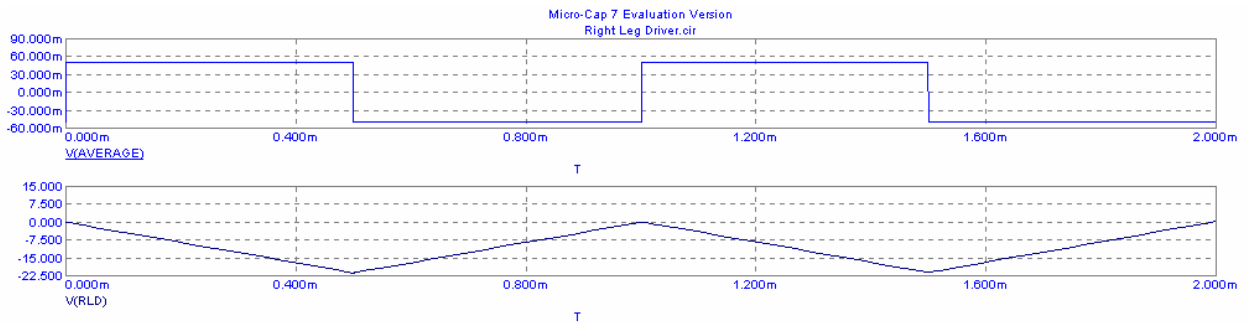
**Figure 15** TI RLD frequency response

When this problem was discovered, the quest for a better model began. After considering many other techniques, the design previously shown in figure 9 was implemented. Using this new model, the same test procedure was attempted. As can be seen, the resultant gain is now in the  $A = 300$  range which is more appropriate for our purposes.



**Figure 16** EPEEA RLD output signal

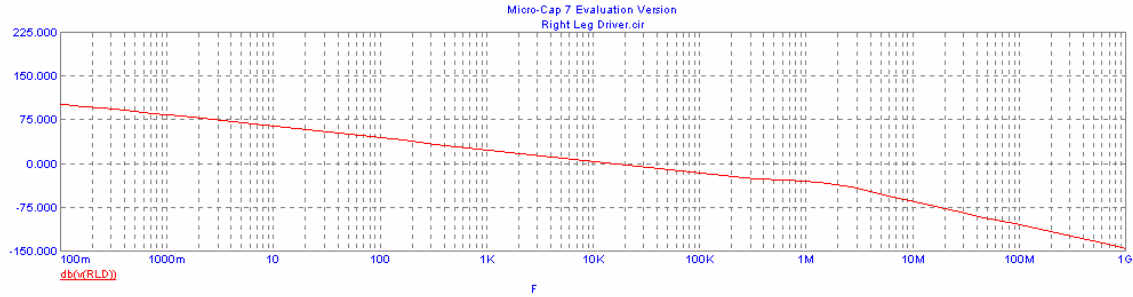
This improved gain was not the reason that this RLD design was chosen however. If one looks closely at the waveform, you will notice that the perfect reciprocity of the input/output signals has been altered. At first one may think that the signal has been merely delayed, but the following figure shows that this is not the case.



**Figure 17** EPEEA RLD output signal

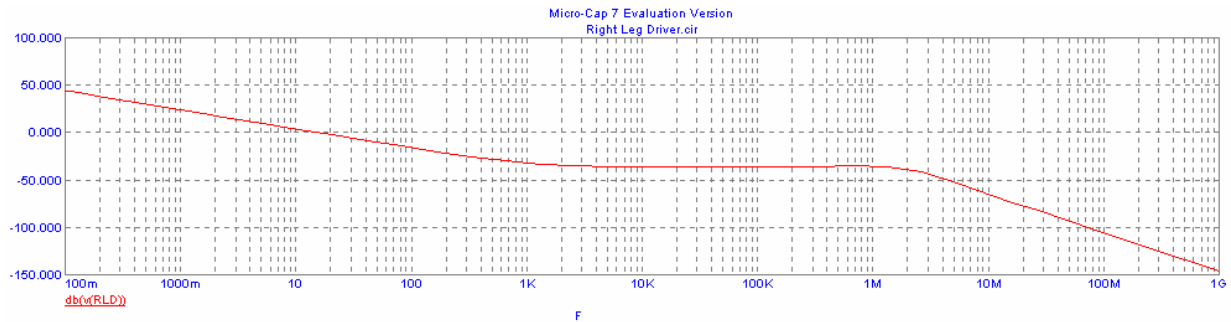
As can be seen, the signal does produce a negative signal at the output, but not in the manner expected. The signal actually continues to increase in potential in response to a constant potential input. This reaction may be beneficial in the following way. If one considers the human body as a variable resistor, the value of that resistor will vary dependent on the two test points chosen. For our purposes, the resistance between COMM and the RLD output will be different if they are both held in the same hand or placed at far extremities from each other. This method of realizing a RLD system ensures that a variable voltage level is used to counteract Interference currents dependent on the resistance between the COMM and RLD signal. If the

electrodes are further apart, a higher gain is initially realized to force the body to the board reference voltage. Furthermore, when the body potential has stabilized, the RLD will force the body to remain at that potential regardless of any outside influences. This nifty little system is only the first reason for using this RLD realization however. It is the frequency roll-off that proves this method to be the best.



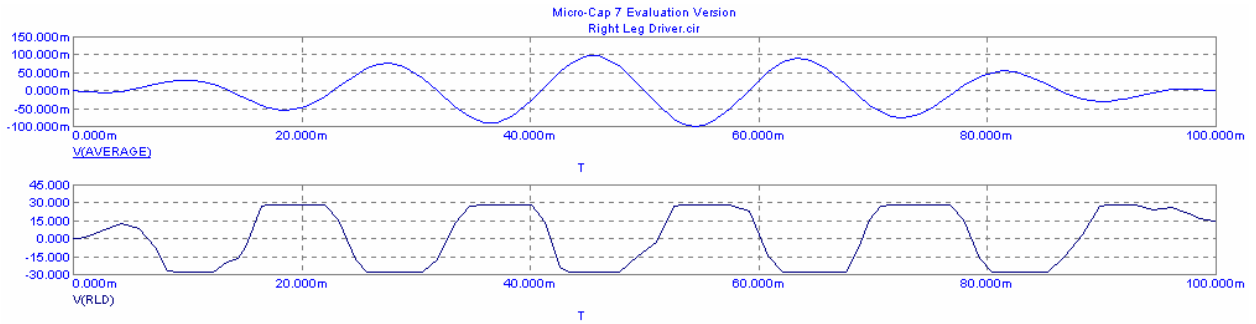
**Figure 18 EPEEA RLD frequency response**

As is shown, the frequency roll-off is substantially better than the TI realization. Whereas, the TI version did not start to reject noise until the 10k mark, this implementation is already at 90dB rejection at that point. This frequency response would not be very beneficial if it were used for any other system than the RLD, but since the objective is to attempt to maintain a constant body potential, the more noise rejection provided the better. This way, a high gain is provided for Gaussian influences of low frequency and the high noise frequencies are rejected. These responses resulted from the EPEEGAG RLD implementation shown in figure 9. The component values in this system were confirmed as follows. The top capacitor (C2) value was both raised and lowered. The response with  $C2 = 1\mu F$  is as follows



**Figure 19 EPEEA RLD frequency response with  $C2=1\mu F$**

As can be seen, the slope does not improve, and the only difference is the location of the first zero, it moves to the left and proves no benefit. When  $C2$  was increased to 100p, the following occurred.

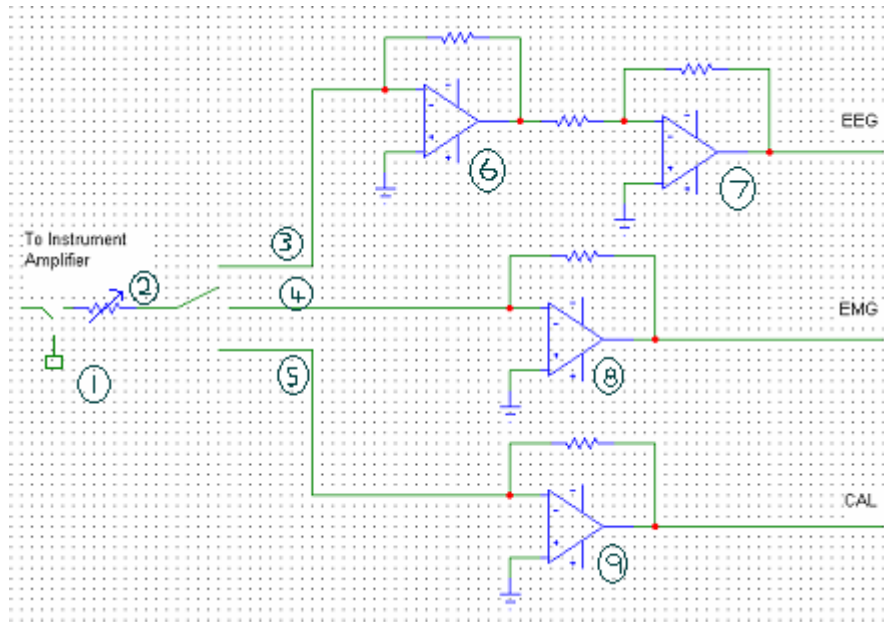


**Figure 20** EPEEAG RLD transient response with  $C2=100p$

The transient response began to rail. This is obviously an unacceptable occurrence, and capacitor  $C2$  was fixed at 1n. Capacitor  $C1$  proved only to relocate the pole location dependent on value, and also ran into the railing issues as above. After further testing, it was found that as long as the capacitors were matched pairs, the frequency response remained fairly similar. The difference provided from using different matched pairs was in the gain, and this worked in tandem with the resistor  $R4$ . The smaller the matched pair of capacitors became, or the smaller the resistor  $R4$ , the larger the gain of the RLD. Since we knew that using a small resistor  $R4$  could lead to oscillation issues in the op-amp, a large resistor was chosen. This value is rather arbitrary since the resistor has very little effect on gain and is used mainly as oscillation protection. We therefore chose a value of 200k, although anything from 10k to 10M would be fine. These tests proved to our satisfaction that the capacitor values were correctly chosen to be 1n each. This value provided the gain of  $A = 300$  which corresponded to our expected Interference currents influences.

#### 5.4 The Mode Switching Amplification Circuit (MSAC)

The purpose of this circuit is three fold: To supply gain for an EEG or EMG signal and to calibrate the gain level with the A/D converter. Although the instrumentation amplifier of the previous stage already boosted the signal by a factor of 30, this second gain stage is needed to condition the signal to fit in the A/D's 3Vp-p input range. The 5K-ohm potentiometer at number 2 in figure 21 Controls the gain of each sub circuit selected by the two pole three throw (2P3T) switch to the right of number 2 on figure 21.



**Figure 21** Schematic of the Mode Switch Circuit

#### 5.4.1 Signal Output Requirements

The output of the MSAC circuit can be no larger than 3Vp-p. This hard upper boundary is to ensure that the signal does not get clipped at the input of the A/D converter. Conversely any signal smaller than 3Vp-p can be amplified to snugly fit the A/D input window. A signal conditioned to the A/D input requirements is guaranteed to use the entire 16 bit resolution range; this will result in the best possible digital representation of the EEG or EMG signal.

#### 5.4.2 The EEG Gain Stage

After the previous differential gain stage the EEG signal can be in a range of 30uVp-p- 4.8mVp-p. So to get the EEG signal up 3Vp-p the gain has to be in a range of 625-100,000. This gain is realized in a two stage inverted operational amplifier configuration. The second stage located at number 7 in 21 Applies a constant gain of 625. The first stage, located just before the second stage, is controlled by the 5k-ohm potentiometer. This stage's gain is in the range of 1-160. With the application of these two gain stages the EEG signal can be easily fit into the A/D's 3Vp-p window.

#### 5.4.3 The EMG Gain Stage

A typical EMG signal is much larger than a typical EEG signal. For this reason a separate gain stage was designed to boost any EMG signal into the 3Vp-p range. An EMG signal coming out of the previous differential amplifier stage can be in a range



of 0.03Vp-p-3Vp-p. The gain of the differential amplifier was designed to boost the largest EMG signal directly to 3Vp-p. This is no coincidence. So the range of the EMG gain channel is 1-100. Only a single inverting operational amplifier stage, controlled by the 5K-ohm potentiometer, is needed to realize this since it is significantly less than the EEG gain. Even though it is not shown on the schematic layout above, a second operational amplifier is used to invert the EMG signal back to the correct phase. This is important to maintain a true representation of the signal.

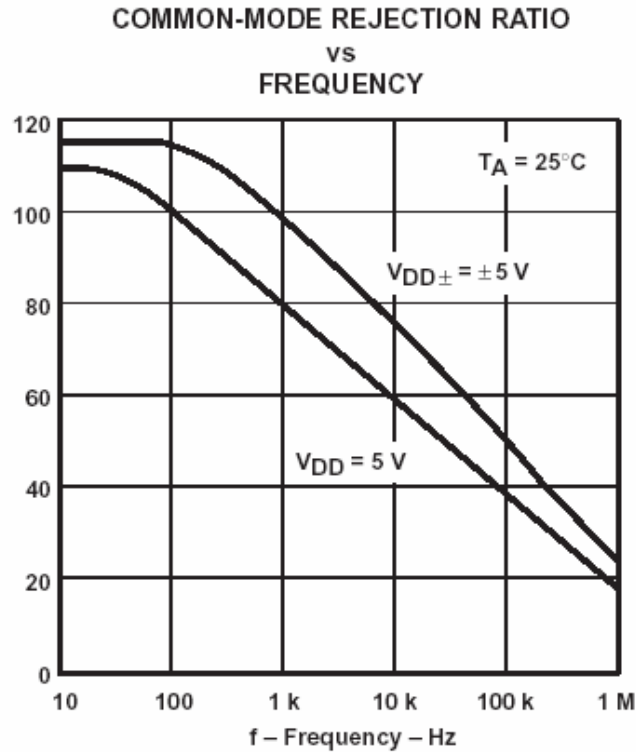
#### 5.4.4 Gain Calibration

The third and final potentiometer controlled gain stage in the MSAC is the calibration stage. The calibration stage is responsible for sending a voltage into the A/D that can be used to determine the position of the potentiometer. The EEG or EMG channel gain can be deduced when the position of the pot is known. The push button located at number 1 in figure 21. Sends a 3V pulse through the calibration gain channel located at the bottom of the above schematic. With the known 3V pulse and known feedback resistor the position or resistance value of the potentiometer can be determined. From here the gain of both the EEG and EMG modes can be calculated. The A/D will simply communicate this voltage through the USB into a computer at which point the gains will be calculated in software.

#### 5.4.5 The TLC2202ACD Operational Amplifier Chip

The TLC2202ACD is widely used in our design. As well as in the MSAC this operational amplifier can be found in use in the Right Leg Driver Circuit. The TLC2202ACD suited our application for several reasons: Single supply operation, 0-5v rail-to-rail output range, and good CMRR.

Since our analog board power supply is 0-5V, single supply is crucial. This means that, the TLCC2202ACD's, +Vcc will be at 5v and -Vcc will be at 0V. The output of the operational amplifier will be centered on 2.5V and since our signal will be only 3Vp-p the maximum output will be at 4v and the minimum will be at 1V. Our signal will not be limited in any way by the operational amplifier's output. Since we are dealing with a very small signal the CMRR is a major factor in determining suitable components. The differential amplifier has a CMRR of greater than 120dB; so much of the noise will be eliminated there. Some noise will still exist in the signal; therefore low noise components must be used in the rest of the circuitry. The TLCC2202ACD has a maximum CMRR of 115dB. The plot below shows the drop off of the CMRR with respect to frequency. This characteristic is great for our application since most of the important information will exist from DC to 100Hz.



**Figure 22** *TLCC2202ACD CMRR vs Frequency Plot*

#### 5.4.6 Passive Components and Channel Cost

The other components in the MSAC, namely the potentiometer, the 2P3T switch and the push button were chosen to provide maximum conductivity of the signals and introduce minimal noise. The 5K-ohm potentiometer has a conductive plastic element and quiet electrical output. The 2P3T switch and the calibration push button have gold plated terminals to provide maximum conductivity to the weak signal.

Taking all of the components into consideration, the 3 operational amplifiers, the 1% resistors, the 2P3T and push button switches, and the potentiometer; the cost to implement a single channel of the MSAC circuit is approximately \$24.

### 5.5 The Digital Backend

The digital section including: filtering, an ADC and a USB communications IC, is present primarily to interface the device signals to a standard digital processing device. In doing so, storage, further processing and analysis will all be possible when


dealing with the observed analog EEG and EMG signals. Because these signals are generated by a biological system they are prone to time transients and short term signal events. This variability makes storage and subsequent analysis an invaluable tool to researchers.

### 5.5.1 General Requirements and Implications

The main requirements of the digital backend are to maintain signal integrity throughout the process while providing data transfer that is reasonably quick with manageable data block sizes. The first concerns in signal integrity are maintaining low levels of noise and minimizing channel-to-channel interference and latency. These issues are specific to the analog to digital conversion step and therefore much of the following discussion concerns the ADC selection process.

### 5.5.2 ADC Selection

~~The noise issue was addressed from several different angles. First, in general, low noise devices were sought.~~ These devices obtained their low levels through various physical and implementation techniques. They tended to be more costly than standard components, thus a great deal of effort was made in finding a suitable trade-off between cost and performance. In addressing their performance the implementation techniques were scrutinized in an attempt to match them with our signal. However, some general requirements, that are known to improve conversion quality, were made first.

- 
1. 16 bit binary code quantization
  2. Low stopband gain (noise floor) in anti-alias filter stage
  3. Inter-channel sample synchronization

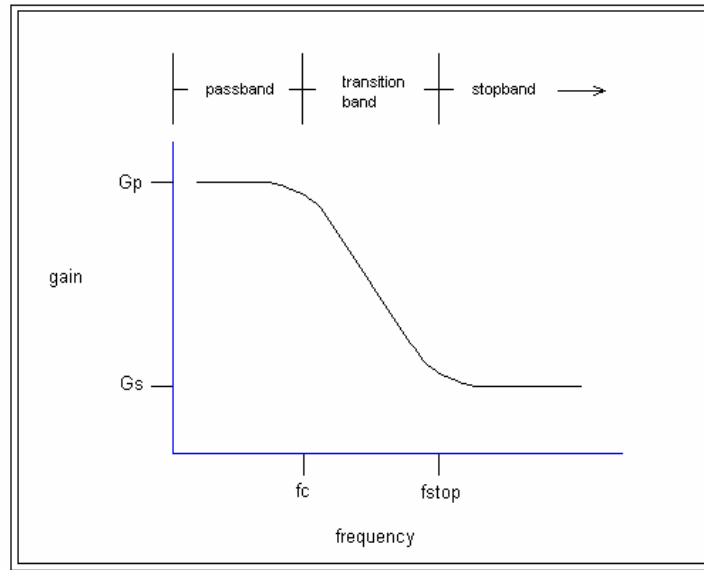
The quantization noise was reduced by requiring 16 bit code output from the ADC. This requirement maximizes the number of available quantization steps thus reducing the error levels. If a linear quantizer is assumed, the following may be said regarding the SNR.

$$\left(\frac{S}{N}\right)_q = 3L^2 = 3(2^{16})^2 = 100dB$$

Where the SNR here is the ratio of peak signal power to average quantization noise power [4].

Next, the stopband gain in the filtering stage is required to be low enough so as to not compromise the high SNR of the analog and quantization stages. The filter of this

stage is an anti-alias filter and thus will have a passband defined by the prescribed bandwidth of the source signal and a stopband that consists of all frequencies from half the sampling rate to infinity. Finally, the transition band is the band in between. In the transition band the gain goes from hi passband to low stopband. Because of this large gain transition, care must be taken to ensure this transition is not over too short a frequency range as the filter order is proportional to the rolloff factor.



**Figure 23** Anti-alias filter response and band definitions

If Nyquist sampling was employed ( $f_s = 2f_c = 2\text{kHz}$ ) then the stopband would begin where the passband ended and a brickwall response with a gain drop from  $G_p$  to  $G_s$  over zero frequency would be required. This would require an infinite order filter; this is obviously unobtainable practically with an analog filter. In response to this problem our sampling frequency was raised.

As defined earlier, our signal bandwidth is 1kHz and our sampling frequency is 8kHz. This gives the following parameters:  $f_c = 1\text{kHz}$  and  $f_{\text{stop}} = f_s/2 = 4\text{kHz}$ , again with a 100dB difference in  $G_p$  and  $G_s$ . The following order calculation was made for a Butterworth lowpass filter implementation [5]:

$$n \geq \frac{1}{2} \frac{\ln \left[ \left( \frac{G_p}{G_s} \right)^2 - 1 \right]}{\ln \left[ \frac{f_{\text{stop}}}{f_c} \right]} = \frac{1}{2} \frac{\ln \left[ (100000)^2 - 1 \right]}{\ln [4]} = 8.30$$

While considerably lower than infinity, this order value is still quite high. With an order this high, concerns regarding phase distortion and implementation cost and size are not trivial. Though other filter realizations (ie Chebychev, elliptic, etc.) may comply with this band disparity more efficiently, the passband ripple of these implementations was deemed counterproductive. The passband ripple would cause distortion that would degrade the signal integrity in the very band of interest thus the Butterworth (maximally flat) response was chosen.

### 5.5.3 Sigma-Delta Modulation as the Solution

At a stage in the project roughly equivalent to where this paper is, the group discovered an ADC implementation known as sigma-delta modulation. This ADC model was immediately attractive for its low order filter requirements, low SNR and reasonable price. The implementation required only that our signal be highly correlated and that a hi clock rate be available to support the oversampling rate. The signal correlation was met in a relative manner. With our signal band-limited to 1kHz and an expected initial sampling rate of 64kHz it was deemed reasonable to assume a relatively hi level of signal correlation over the time of a sample period. In addition, the clock speed was already available as part of the USB communications system implementation.

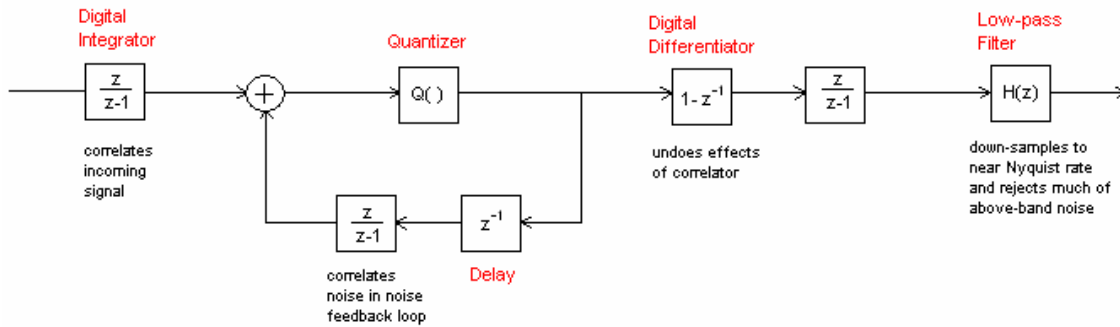
A particular ADC was chosen from Analog Devices (AD73360) because of its high channel capacity, programmable flexibility and cascading option. The device comes in a standard six-channel configuration. Though this does not satisfy the ten channels the project required, the option to cascade the serial data streams of multiple devices allowed for an “effective” ten-channel device to be configured. In addition to satisfying the channel requirements the channel sampling was stated as being highly synchronized which would ensure minimal channel latency. Finally, there were several peripheral advantages to the AD73360. The device offered the following programmable parameters:

- Variable sampling frequency
- Variable input gain
- Input inversion
- Variable output serial data rate
- Differential or absolute inputs

In addition, this device has low power consumption (80mW) and requires much less physical space for implementation on a PCB.

Sigma-Delta modulation employs clever techniques in order to reduce the order of the antias-filter while maintaining low noise output. First, it must be recognized that the noise due to quantization of an ADC will be focused in the frequency band from DC to  $f_s/2$  and will have decreasing spectral density with increasing sampling frequency.

Therefore, the first step in the sigma-delta scheme is to sample at a rate much higher than the required Nyquist rate. This greatly reduces the amount of inband noise and relaxes the rolloff requirements of the analog anti-alias filter (so much so that a single pole RC filter is generally sufficient). Next, quantization noise approximations from past quantization steps are fed back to the incoming signal in order to further limit the introduced noise. This step requires that the successive samples are similar in magnitude thus motivating the high correlation requirement mentioned earlier. This step effectively pushes noise out of the signal bandwidth into an above band region that will eventually be filtered out. The next step of the scheme is to employ a hi-order sinc cubed filter that simultaneously reduces the sampling rate (to a rate that approaches the Nyquist rate) and rejects much of the out of band noise. The diagram below illustrates a general implementation of sigma-delta modulation.



**Figure 24** Signal graph of sigma-delta modulator [4]

The transfer function of the above signal flow graph is given by:

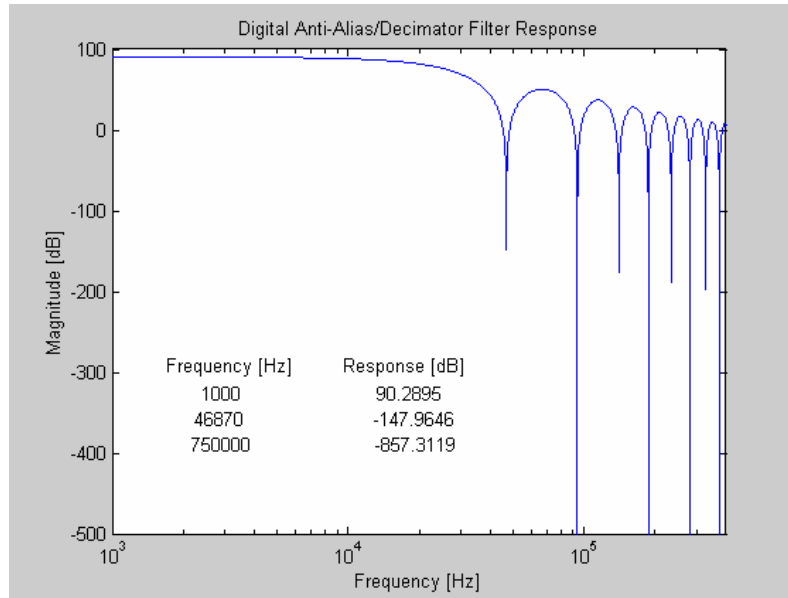
$$Y(z) = X(z) + Q(z) \frac{z-1}{z}$$

Where  $Q(z)$  is the z-transform of the quantization noise fed back to the input. The important thing to notice is that the process does not affect the source signal but acts as a differentiator to the noise [1]. This is equivalent to a high-pass filter “pushing” the noise out of band.

The last part of the scheme is the low-pass reconstruction filter. This filter transfer function was given for the AD73360 as follows:

$$\frac{Y(z)}{X(z)} = \left[ \frac{1 - z^{-32}}{1 - z^{-1}} \right]^3$$

The frequency response of this filter is shown on the following page. This filter decimates the initial sampling by a factor of 32 and rejects the quantization noise pushed into the upper lobes of the response. There is one last filtering stage that is required and that is a customer implemented low-pass anti-alias filter. This final stage will further reduce the sampling rate (for this project  $f_s \approx 8\text{kHz}$ ) to the desired level and provide the final stage of noise rejection.



**Figure 25** Decimation filter magnitude response

#### 5.5.4 Serial Data Interface

Now that much of the details of the digitization have been addressed, some minimal reference will be made to the handling of the serial data stream from the ADC section. First, it should be noted that there is little to no “overhead” data in the serial data from the ADC. Separate control lines to and from the device handle any communications control. With this in mind the overall bit rate may be determined as follows:

$$\left(16 \frac{\text{bits}}{\text{sample}}\right) \left(8000 \frac{\text{sample}}{\text{sec} \cdot \text{channel}}\right) (12 \text{channel}) = 1.54 \text{Mbps}$$

This represents the minimum bit rate required for the parameters prescribed thus far. In addition to this data rate there are some minimal control signals required in order to operate the ADC serial port. These signals consist of enables and framing signals and do not pose any serious difficulty in providing for.

### 5.5.5 USB Communications IC

Because of time constraints and shipping problems, little development work was done on this phase of the project. For this reason, only the basic specifications will be addressed for the USB device.

The USB device chosen is the Cypress EZ-USB FX2™ USB Microcontroller (CY7C68013). This device integrates a USB 2.0 transceiver, 8051 microcontroller and a programmable peripheral interface on a single chip. The specifications allow for data rates up to 56Mbytes per second (as per USB 2.0), which will be sufficient for the serial data rate derived above. The peripheral communications are by way of a general programmable interface (GPIF) or a master/slave FIFO register scheme. These options will accommodate exchange with our ADC directly or with a standard DSP. The cost of a single EZ-USB chip is \$34 CDN. Only one is required for the EPEEA system.

## 5.6 Board Power

Due to power requirements of the board components, the board is divided into three main power planes. These are the ground plane (AGND), the power plane (ABATT) and the reference plane (BUF\_REF). As well as these power planes, there also exist three distinct power sections. These are the analog, digital and computer power section.

### 5.6.1 Power Planes

The single supply operation of the ADC was the driving factor in the decision to use a single supply rail. Initially, the board was designed so that it would operate with both a positive and negative rail, using the ground as the reference. This design was implemented and produced accurate signals using an oscilloscope for retrieval purposes. However, once the ADC system was fully researched, it became apparent that any methods implemented would require the signal to be re-referenced to the ADC input values. It was decided that the use of a single rail system would be more efficient than a dual-rail system coupled with a re-reference system. Also, the ADC chosen provided a BUF\_REF signal that produced a reference voltage in relation to the differential inputs provided to the ADC.

Due to the requirements of the ADC, the following voltages were chosen. The ground plane is obviously our zero reference voltage. The power rail is at +5 volts, and the BUF\_REF provided by the ADC is approximately 2.5 volts. These voltages are now used to operate all of the active components of the board.

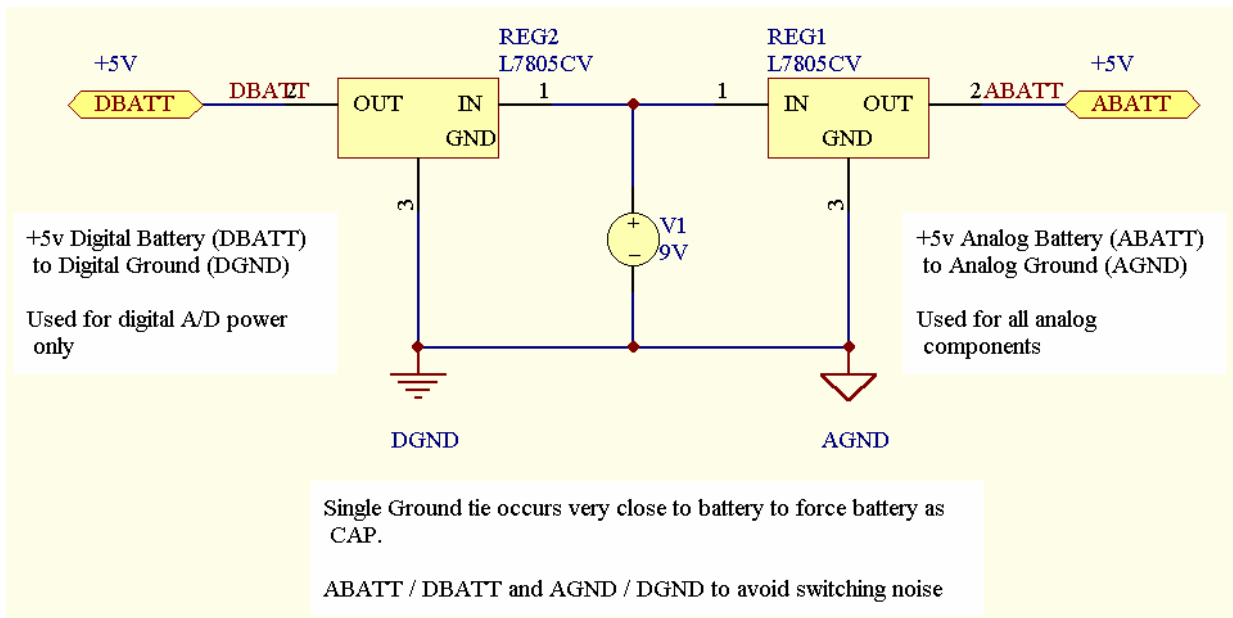


For the op-amps, the power supplies are 0 and +5 volts. This results in an output voltage fluctuating around 2.5 volts. The same can be said for the instrumentation amplifier which also has the added benefit of an available pin that inputs the reference voltage, BUF\_REF, which causes the output to fluctuate around this voltage. This added feature allows for minor fluctuations in the BUF\_REF voltage to be compensated for in the instrumentation amplifier so that the ADC will produce accurate differential conversions.

A 9-12 volt battery and 5 volt regulator system is used to achieve the power plane. Batteries were used to ensure that the power provided is extremely reliable and free of noise.

### 5.6.2 Power Sections

The three main sections of the board can be summarized as follows. The analog section of the board receives analog power, ABATT and AGND, from the battery system. The BUF\_REF signals also operate in this section. The digital section of the board receives digital power, DBATT and DGND, from the battery system. This section includes the ADC's and the optocouplers. AGND and DGND are connected in only one location, near the batteries, to ensure like potentials. The reasoning for this connection location is that being near the batteries, any switching frequencies found on the digital side of the board are fed through the batteries as they act as infinite capacitors. The schematic connection can be seen below.



**Figure 26** Power schematic

The final power system of the board is confined to the USB and the digital side of the optocouplers. These components require computer power to operate, which is provided.

## 5.7 Board Layout

The schematic layout of the EPEEA design has been fully realized in Protel. These schematic drawings include the footprint models and construction documentation. Many of these schematics can be found on the EPEEAG website, [www.engr.uvic.ca/~duddenbe/index.html](http://www.engr.uvic.ca/~duddenbe/index.html), including a 3D representation of our completed 10 channel system.

Originally, the device was modeled in Protel using through-hole components and a four layer board. These four layers were positive plane, ground plane, reference plane and component plane.

Due to the high cost of producing four layer boards, the system was redeveloped using only two planes. These are the power and ground planes. Although the two planes would normally lie above each other in order to mimic a capacitor and thereby reduce noise effects, the power plane must also accommodate the reference signal as well as the components, which makes this no easy task. So, due to these space

constraints and the antenna-like effect of through-hole components, the entire system was redesigned using surface mount components only. This new design required significant development time due to multiple issues such as track layout, footprint construction, ground plane layout, RF filter development, space constraint and many others.

The overall PCB dimensions are approximately 11"x10" for the ten channel version. A smaller six channel version is possible, as well as a dual-six, twelve channel version which is being developed. The approximate cost for such a large PCB board is \$500 for the first printing with costs reducing significantly for multiple boards.

## 5.8 Implementation Cost

The following table shows the cost breakdown of building a prototype EPEEA system.

Subsystem	Cost per Channel	# of Channels/Items	Full Cost
Protection CKT	1.6	10	16
Instrum. Amp	25	10	250
RLD	6	1	6
Mode Switch CKT	24	10	240
A/D	15	2	30
USB	25	1	25
Power	15	1	15
PCB	500	1	500
Box	50	1	50
Misc	100	1	100
		<b>TOTAL</b>	<b>\$1,232</b>

The budget of \$1000 has been exceeded by only \$232. The most expensive part of building this unit is the cost of the printed circuit board (PCB) production. Since this is the first one to be built, most of the PCB cost is spent on template construction. Consecutive, non-prototype systems could be easily built under \$1000. The miscellaneous costs can be attributed to underdetermined components such as wires, connectors and electrodes.

## 6.0 Conclusions

The goal of this project was to design and build a 10-channel Experimental Portable EEG/EMG Amplification (EPEEA) system. Funded by the University of Victoria's Assistive Technologies group (UVATT), the EPEEA was designed to obtain data up to 1000Hz with a budget constraint of \$1000 CDN. Traditional systems on the market similar to this one have limited bandwidths and tend to be quite expensive. However, current, state of the art EEG/EMG amplification systems were researched to obtain the specifications for the EPEEA. Further information regarding specifications were found on the internet, particularly the OpenEEG user community.

The EPEEA has six sub-systems that work in conjunction to detect an EEG/EMG signal, amplify it, digitize it, and finally create a USB data stream that can be read into a personal computer. The cost of the overall system, including board manufacturing, came to approximately \$1,232 CDN. The term approximately is used because component prices tend to fluctuate between different distributors. This total cost exceeds the original goal of \$1000. However, the cost of prototyping a PCB design is much more expensive than re-creating a board off an existing template. The non-prototype EPEEA system could be built for \$1000 CDN.

The initial goal of the project was to build the EPEEA as well as design it, however many obstacles in the way prevented group 11 of the 499a class from completing a finished unit in 3 months. Much research in to the background of EEG and EMG had to be done before embarking on the design. Once designed, much time was spent ordering and waiting for parts to come from various manufactures and distributors. The EZ-USB with the development kit did not come until near the end of the semester. However, for demo purposes, a single channel of the EPEEA was implemented and tested.

In the near future the EPEEA system will be fully built and tested by the UVATT group. Furthermore, software will be developed to analyze and process the EEG/EMG data, which will be used to set up a control interface to a PC for 'locked in' persons.

## 7.0 Recommendations

Even though our system design has been completed and tested with a one channel prototype module, there are some things that still need to be completed with the existing system:

- Obtain the full, 10-channel printed circuit board (PCB) of our design with all surface mount components.
- Complete the USB section of the design with control for the A/D converter.
- Research and implement a DSP chip between the A/D converter and the USB chip for increased filtering.

- Complete a proper “break-out box” for electrode cables to be interfaced to.
- Build a proper RF isolation box for our circuit board.
- Design and implement the graphical user interface (GUI) to be used by the researchers. This would consist of a time and frequency domain representation of our signal.

With these recommendations completed, and research testing underway, a new wave of recommendations and system improvements would become known.

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# APPENDIX I

## Interference and the Right-Leg Driver (Driven Right Leg)

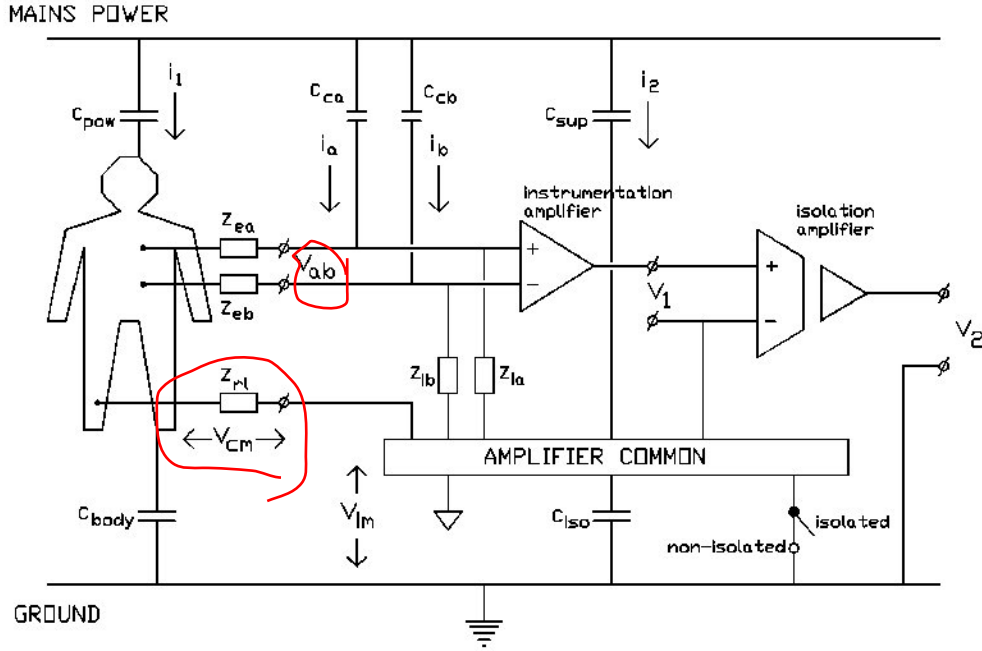
This article is a conglomerate of various papers textbooks and observations intended only as an instruction tool for our product development. For full text, please visit the sources.

### 1. Introduction

~~Bioelectric recordings are often disturbed by an excessive level of interference. Although its origin in nearly all cases is clear - the mains power supply (high level 120V 60Hz voltage) - the cause of the disturbance is not at all obvious because in many cases very sophisticated equipment is used.~~

### 2 Interference

The capacitances between the patient, the power lines and ground cause a small interference current to flow through the body (see Fig. 1). In the modeling of the measurement situation the capacitance between the body and ground ( $C_{\text{body}}$ ) is taken to be 300 pF and the capacitance between the body and the mains power ( $C_{\text{pow}}$ ) is taken to be 3 pF (Huhta and Webster, 1973; Forster, 1974) which values can be assumed to be typical. In other words, the patient is not grounded at all. These capacitances cause an interference current ( $i_1$  in Fig. 1) of about 0.5  $\mu\text{A}$ ,p-p to flow from the power supply lines (220 V,rms, 50 Hz (Europe)) through the body to ground. If an amplifier is connected to the patient, part of the current from mains to patient ( $i_1$ ) will flow to ground through  $Z_{rl}$  - the impedance of the electrode-skin interface of the "neutral" electrode (the right leg electrode in standard ECG measurements). The portion of  $i_1$  that flows through  $Z_{rl}$  causes a potential difference between the average potential of the body and the amplifier common: the common mode voltage ( $V_{\text{cm}}$  in Fig. 1).



**Figure 1:** Floating ground representation for a human

Another major source of interference in bioelectric measurements results from the capacitive coupling of the measurement cables with the mains ( $C_{ca}$  and  $C_{cb}$  in Fig. 1). The currents induced in the wires ( $i_a$ ,  $i_b$  in Fig. 1) flow to the body via the electrodes and from the body to ground via  $C_{body}$  and via  $Z_{rl}$  in series with  $C_{iso}$ . Because both the currents induced in the wires and the electrode impedances generally differ significantly, a relatively large differential voltage is produced between the amplifier inputs ( $V_{ab}$  in Fig. 1). The magnitude of this voltage is given by the following relation:

$$V_{ab} = i_a Z_{ea} - i_b Z_{eb} = i Z_e \frac{dZ_e}{Z_e} + \frac{di}{i} \quad (1)$$

$$\text{where } i = \frac{1}{2}(i_a + i_b); \quad Z_e = \frac{1}{2}(Z_{ea} + Z_{eb})$$

A typical situation with a mean current of 10 nA,p-p in the wires, a mean electrode impedance of 20 k-Ohm and a relative difference in interference current and electrode impedance of 50%, leads to an unacceptable high interference level of 200 microV,p-p.

These values are taken directly from an article, and do not relate exactly to our application, but it is obvious that this issue must be addressed.



Aside from these two sources, there are also various other sources of interference including current into the amplifier and magnetically induced interference. These sources are not as significant but will be addressed.

### **3. Reduction of interference currents in the measurement cables**

Given the inherent variability of the electrode impedances and the level of interference among recordings (Eq. 1), there is only one practical way to reduce interference currents in the wires: shielding of the measuring cables. The different possible shielding techniques are treated in the following.

1) Shields connected to amplifier common Simply connecting the shields to the amplifier eliminates interference currents in the wires. However, it usually does not reduce the total level of interference. The high capacitance of shielded input cables reduces the input impedance of the amplifier resulting in an increase of the level of interference because of the potential divider effect (Eq. 3). The common mode signal, which is the cause of this form of interference, can not effectively be reduced with a driven right leg circuit because the increased input capacitance of the amplifier easily results in instability of the circuit.

2) Guarding When a shield is driven with the signal at the inner wire, there is virtually no cable capacitance and its contribution to the input impedance of the circuit is negligible (Morrison, 1977). This technique is usually known as guarding. A consequence is that for each input an extra amplifier is needed to drive the shield.

3) Guarding with the average of the input signals If all shields are driven with the average of the input signals (= common mode voltage), the input capacitance for common mode signals is virtually small because there exists no potential difference between shield and inner wire for these signals. Hence, there is no extra sensitivity to interference signals caused by the potential divider effect. Stability problems of an effective driven right leg circuit can be avoided with a careful design of the guarding circuit. This method is a good compromise between the other two shielding techniques: good interference suppression is achieved with just one extra amplifier. A drawback is that the input capacitance for differential signals is just as low as in the situation with the shields connected to the amplifier common because for differential mode signals the voltage difference between shield and inner core is not reduced by the guarding circuit. The resultant low input impedance for differential mode signals at high frequencies may lead to signal loss and distortion (Geddes and Baker, 1966b). However, in normal ECG and EEG recordings which have a restricted frequency content ( $< 200$  Hz), the extra input capacitance for differential mode signals is not problematic if extremely long measuring cables are avoided.

Guarding circuit Both shields are driven by the same buffer amplifier. This buffer should have a gain of unity from DC up to a few MHz in order to assure stable operation of the complete amplifier. Some operational amplifiers used in a buffer configuration have a gain larger than unity at high frequencies. Proper compensation should be provided in these cases because of possible instability.

The input signal for the shield driver should be the average of the input signals. A good approximation of this signal is the average of the inverting inputs. To compensate for the capacitance of the inverting input of the input-operational amplifier, small capacitors ( $C_f$ ) with a value equal to the input capacitance must be added (see Fig. 3). The gain of the shield driver has been put to 0.99. This reduces the signal magnitude at the shield to 99% of the average signal magnitude at the inner wires thereby improving the stability of the guarding circuit and reducing the peaking in the frequency response, while there remains a considerable reduction of the effective cable capacitance (a factor 100) (Morrison, 1977).

#### 4. Influence of common mode voltage

There are two ways by which a high common mode voltage may cause interference. The first, obvious way is when the common mode rejection ratio of the amplifier is limited. This mechanism is not often problematic with modern differential amplifiers: a common mode rejection ratio of 80 - 90 dB is customary. A second, and much more important way a high common mode voltage may cause interference is when there are differences in electrode impedances and/or input impedances which convert common mode voltage into a differential input voltage (see Fig. 1). This mechanism - often called "the potential divider effect" (Huhta and Webster, 1973; Pacela, 1967) - is the main reason why it is important to reduce the common mode voltage as much as possible. The magnitude of the differential interference input-voltage generated this way, is given by the following relation (see Fig. 1):

$$V_{ab} = V_{cm} \frac{Z_{ia}}{Z_{ia} + Z_{ea}} - \frac{Z_{ib}}{Z_{ib} + Z_{eb}} \quad (2)$$

where  $Z_{ia,b}$ : input impedances

$Z_{ea,b}$ : electrode impedances

It is instructive to rewrite this equation assuming the input impedances to be much larger than the electrode impedances:

$$V_{ab} = V_{cm} \frac{dZ_e}{Z_i} \left( \frac{dZ}{Z_e} + \frac{dZ_i}{Z_i} \right) \quad (3)$$

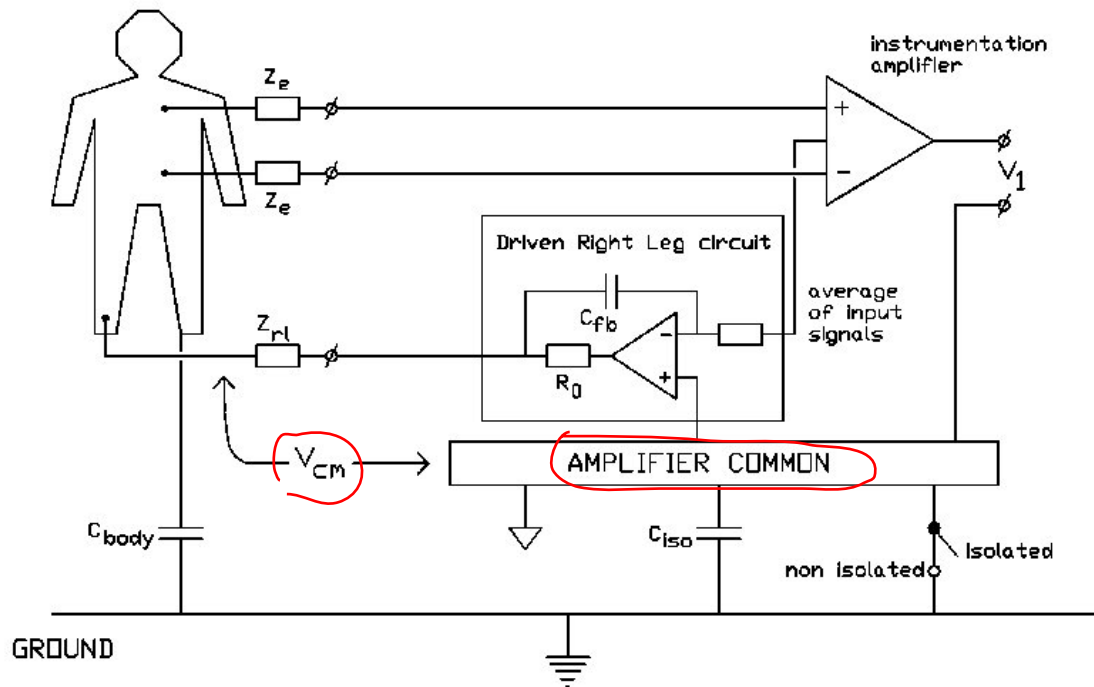
$$\text{where } Z_e = \frac{1}{2} (Z_{ea} + Z_{eb}), \quad Z_i = \frac{1}{2} (Z_{ia} + Z_{ib})$$

It appears that the level of interference generated by the potential divider effect depends on the magnitude of the common mode voltage, the ratio of the average electrode and input impedances, and on the relative differences in electrode and input impedances. The usual electrodes may show a mean impedance of 20 kOhm at 50 Hz and impedance differences of ca. 50 % (Almasi and Smitt, 1970; Grimnes, 1983; Geddes, 1972).

Differences in input impedances should not exist in a carefully designed amplifier system, but often these differences are not easy to avoid. Differences in input impedances are often found in multi-channel measuring systems but may also be caused by the use of shielded input cables of different length.

### **5. Reduction of the common mode voltage**

A proper driven right leg circuit (see Fig. 2) offers a large reduction of common mode voltage magnitude in both isolated and non-isolated measurements by actively reducing the voltage difference between patient and amplifier common; a reduction between 10 and 50 dB is usually accomplished. A driven right leg circuit is the most practical way to reduce the common mode voltage if a reduction of interference current through  $Z_{rl}$  is not feasible. In addition, the driven right leg circuit makes measurements reasonable safe in a non-isolated situation (switch closed in Fig. 1 and Fig. 2) because a rather large impedance between body and ground can be achieved by selecting a large resistor  $R_0$  (several MOhm) and a small feedback capacitor  $C_{fb}$  ( $< 1$  nF). This feature can be used to omit isolation amplifiers in experimental situations in which safety standards are not as critical as in clinical situations. The main drawback of a driven right leg circuit is it being potentially unstable (Winter and Webster, 1983). In practical designs, a compromise between common mode suppression and possible instability - depending on circumstances - must be found.

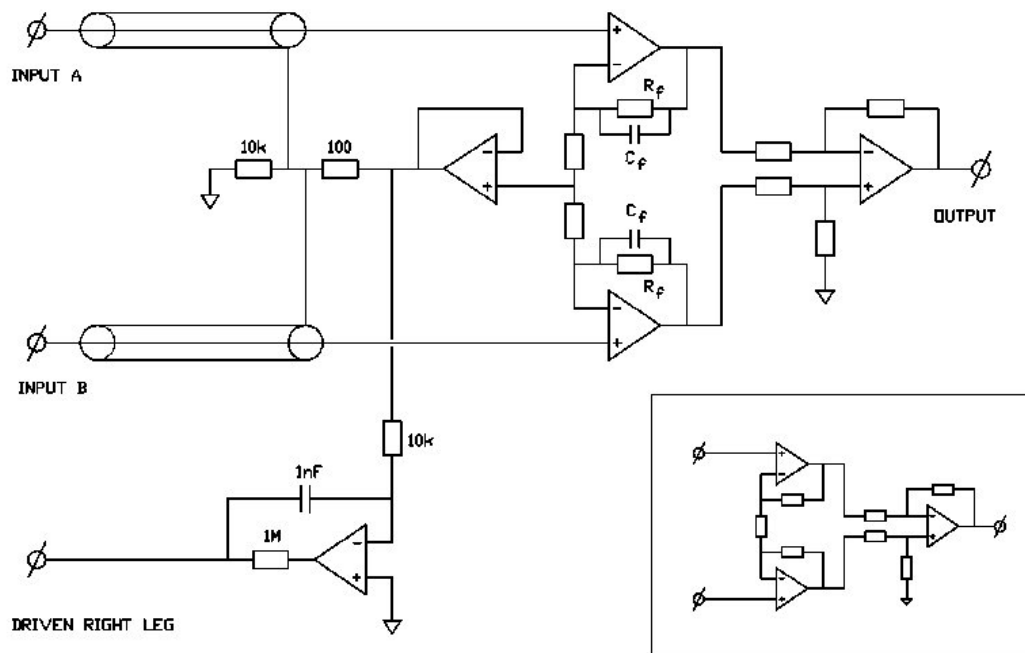


**Fig.2** Driven right leg circuit. If the gain of the driven right leg circuit is high, the common mode voltage ( $V_{cm}$ ) is much smaller than the voltage across  $Z_{rl}$ .

## 6. Design of a Driven Right Leg System

Driven right leg circuit The input signal for the driven right leg circuit should be the average of the input signals (= common mode voltage). The output signal of the shield drive buffer differs very little from this average signal for reasons described above, and can be used for this purpose. The open loop gain of the driven right leg circuit is 300 at 50 Hz resulting in a 50 dB increase in common mode rejection at this frequency. This proved to be a good compromise between maximum common mode reduction and stability requirements.

For reasons of simplicity, the low frequency roll-off is not shown in the circuit of Fig. 3. In practical use the amplifier should have a low gain for DC signals to prevent saturation caused by electrode off-set voltages to occur. There are several solutions for DC suppression (Hamstra et al., 1984; McClellan, 1981).



**Fig.3** Biomedical instrumentation amplifier equipped with guarding and driven right leg circuits, based on the three operational amplifier instrumentation amplifier (see inlay).

Instrumentation amplifiers consist of two unity gain pre-amp op-amps and a differential amplifier. When the negative inputs for the pre-amp op-amps are tied together via resistors, a floating ground is created. This floating ground is the reason that the differential amplifier can achieve such high CMRR values. The pre-amp op-amps act as voltage followers (due to the floating ground) and the common-mode gain equals 1. The capacitors shown in the above picture,  $C_f$ , should not affect the DC component of the signal.

$$A_v = R_2/R_1 + 1$$

$$A_{cm} = 1$$

Remember,

$$CMRR = A/A_{cm}$$

So obviously, a  $A_{cm} = 1$  is as good as we could hope for!

Now, the second stage controls the gain and the CMMR

Due to the rules of a differential amplifier, this system acts like a wheatstone bridge. The difference in the four resistors becomes system downfall. The gain  $A_v = 1$  as all of the resistors are of the same value, and the common-mode gain  $A_{cm} = \pm 2 \Delta R/R$ .

The issue then becomes how closely matched the resistors can be. For example, for 10000 ohm resistors that are  $\pm 0.1$  percent, the CMRR becomes a minimum of 54dB, for

$\pm 0.01$  percent, it becomes a minimum of 74dB. All of these issues are fixed with the introduction of the INA114BP IC chip, it has a gain of 10000, and a CMRR of 115db (CMRR  $\cong 562000$ ), which means, the resistors must be within  $\pm 8.89 \times 10^{-5}$  percent of each other! We will never be able to find resistors of this accuracy, which leads me to believe that they are using an alternate method. I say, go with the chip.

Now, the floating ground becomes the issue.

A DRL circuit reduces the common mode voltage by actively driving to the potential of the amplifier common (MettingVanRijn et al., 1990). A DRL, in addition, protects the patient from the consequences of amplifier defects because a series resistor in the circuit ( $R_0$  in Fig. 2) limits the maximum current through the ground electrode to a safe level. The common mode suppression of a DRL circuit increases with decreasing frequency. Consequently, the DRL circuit compensates for the decreasing CMRR of the instrumentation amplifier at low frequencies. In our view, a DRL should be used in every biomedical recording system for interference suppression and patient safety. Therefore, when the instrumentation amplifier is compared with other designs with respect to the needed number of parts, the DRL circuit should not be regarded as a particular complexity.

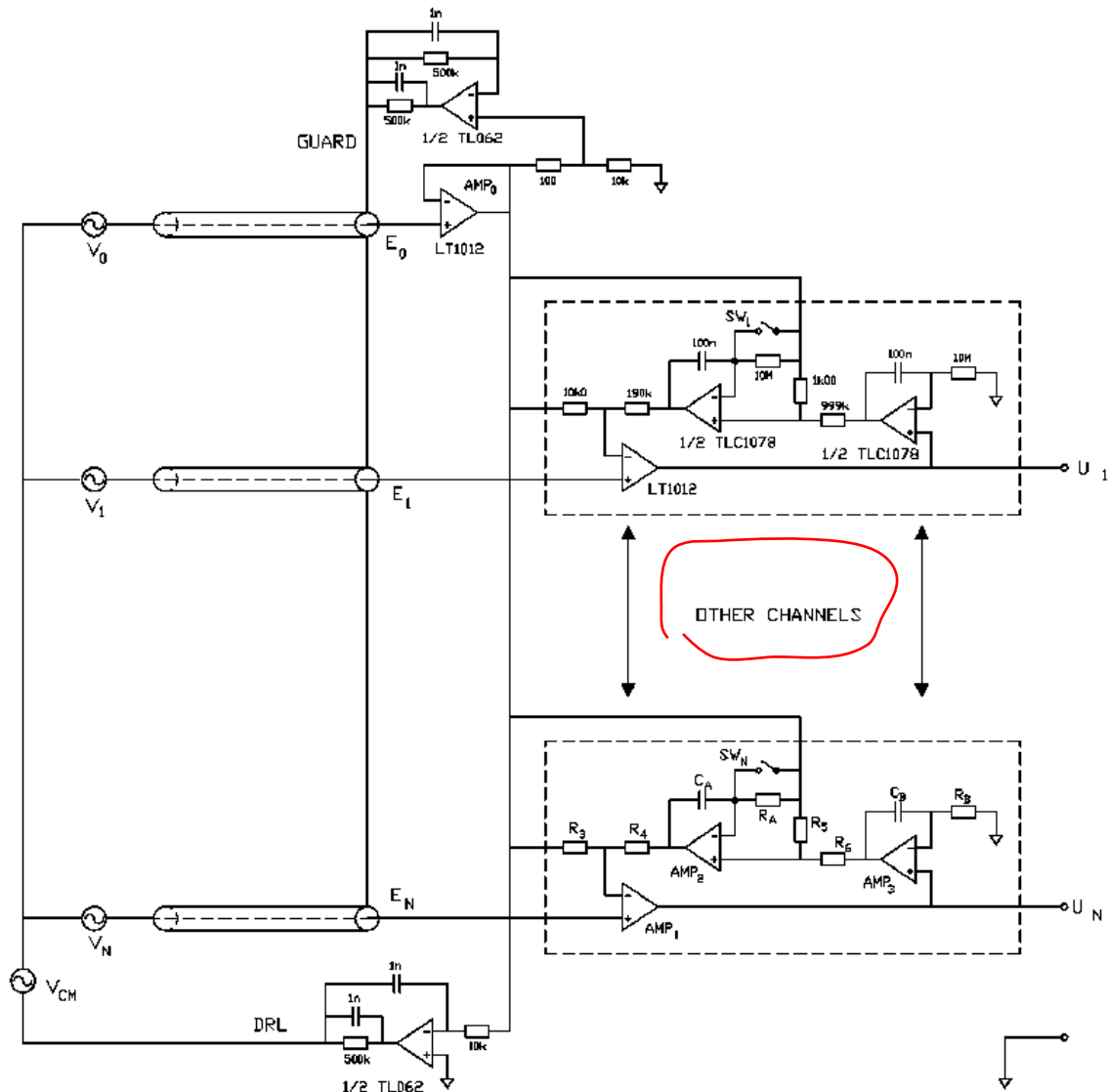
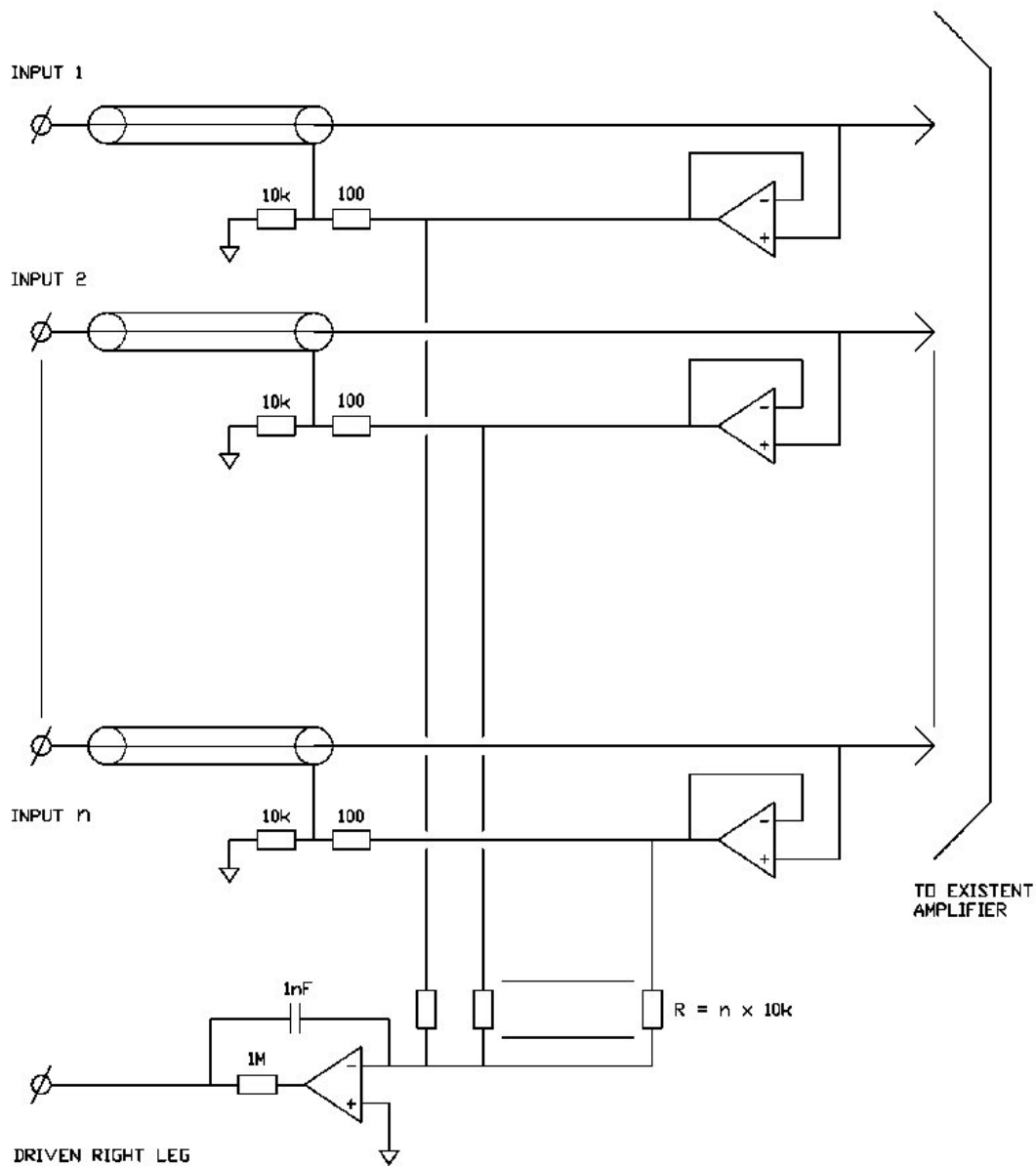


Figure 4: A typical Driven Right Leg System

## 7. An add-on device for a recording system

If the performance of a recording system is poor and the development of a complete new amplifier system can not be considered, use can be made of the circuit shown in Fig. 5. This circuit can be added to any amplifier. It suppresses common mode voltage effectively and it provides guarding of the measurement cables without deteriorating the performance of the existing amplifier. The extra input capacitance and bias current can be neglected when high quality JFET operational amplifiers are used. The circuit can be extended to any number of channels. The device is in use for the recording of surface His-bundle potentials (Peper et al., 1985) where very small signals (some microvolts) have to be recorded and a low level of noise and interference is of utmost importance.



**Fig.5** Add-on circuit for a n-channel bioelectric measurement. The circuit reduces the common mode voltage (driven right leg circuit) and interference currents in the measurement cables (guarding).